Effects of High-k on FinFET Performance

Fatin Syamila bt. Mohammad
Faculty of Electrical Engineering, Universiti Teknologi MARA (UiTM),
40450 Shah Alam, Malaysia.
fatinsyamila@gmail.com

Abstract – **Scaling down transistor to 45nm node and below might require new processing steps such as new gate stack or new device structure such as FinFET. Thus, in this work the use of high-k gate insulator - hafnium oxide (HfO_2) on FinFET performance was investigated. SPICE model was used to describe the real device operation and designing a practical analog circuit for the AC analysis. Therefore, only the gate insulator is changed in the SPICE model of silicon oxide, SiO_2 to HfO_2 and the difference of the turn on current (I_{ON}) is compared between planar and FinFET SiO_2 gate insulator with HfO_2 gate insulator FinFET transistor. The simulation results for 22nm node on inverter and chain inverter application show that better performance was obtained for FinFET compared to planar bulk CMOS.**

Keywords – FinFET, high-k, hafnium dioxide

I. INTRODUCTION

As the dimension of a transistor shrinks, the transistor becomes smaller, lighter, faster, consumes less power and in most cases more reliable [1]. Thus, two types of transistor structures – conventional planar and tri-gate transistors will be examined. Tri-gate transistors make use of a raised source-drain structure that would eliminate parasitic resistance and at the same time facilitates local interconnection and large-scale integration [2]. The purpose of this study is to resolve the problem of current leakage by using high-k gate in tri-gate transistor. Silicon oxide (SiO_2) is ideally an insulator but as transistor is made thinner, current will leak through. Hafnium oxide (HfO_2) with the dielectric constant about 30 (k_{HfO_2}≈30) is a much higher value of insulator gate that is being used to replace the currently used SiO_2 gate with the dielectric constant of 4.3 (k_{SiO_2}=4.3) [3]. High-k gate dielectric materials were employed in the process to continue the scaling down of transistors at low gate leakage [4]. The usage of high-k/metal gate offers a very significant gate leakage reduction relatively to 65nm transistors [5] as the gate leakage is reduced by more than 25 times for nMOS and by 1000 times for pMOS compared to the transistor that uses poly-Si as the gate [6]. Software called LTspice will be used to compare planar and tri-gate transistor by varying the k value. Other parameters are kept constant. Higher value of k in insulators can be grown physically thicker or thinner for the same electrical oxide thickness (t_{ox}) that shows an apparent reduction in the gate leakage. The high-k/metal gate FinFET uses 1.9nm as the oxide thickness that uses HfO_2 as the gate insulator. However, FinFET with poly-Si gate uses 1.8nm as the oxide thickness with SiO_2 as the gate insulator.

II. METHODOLOGY

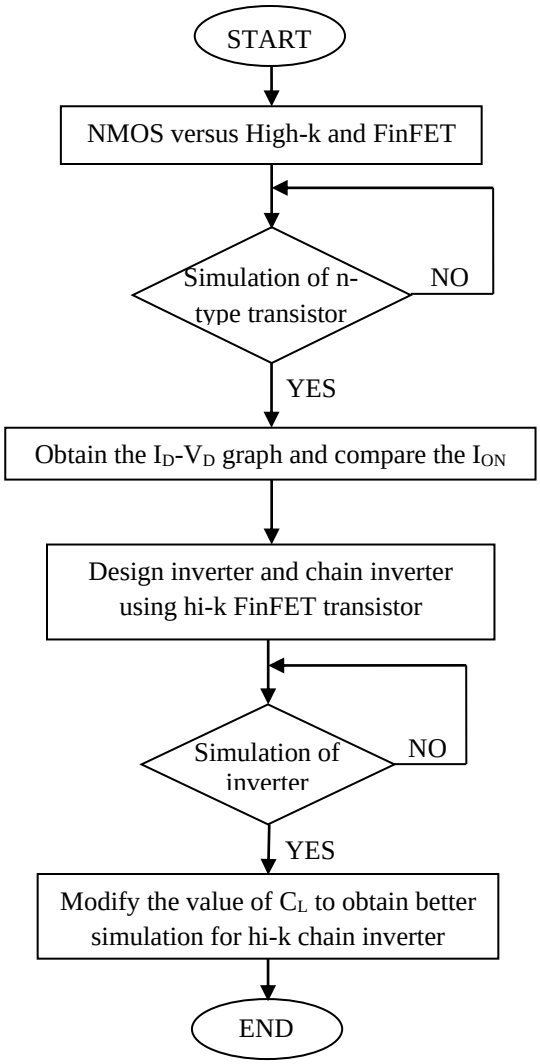


Figure 1: The flow chart of the overall simulation work

Figure 1 shows a flow chart of the overall work of designing transistor and two types of transistors is being compared. The simulation was performed to investigate the effect of high-k on FinFET performance. The comparison was made between n-type MOS and FinFET transistor in 3D model, I-V characteristics and as an inverter. Then further simulations were performed to examine the effect of high-k FinFET for chain inverter.

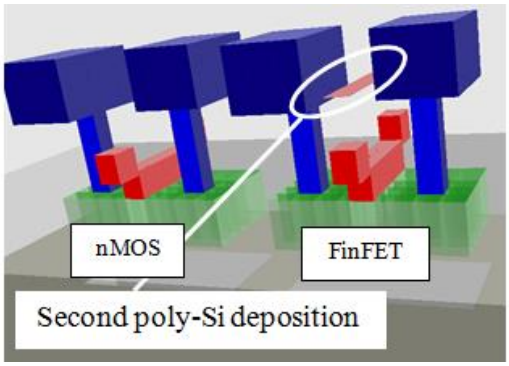
In this simulation, the values either the dielectric constant or electric permittivity (ε_r) cannot be modified directly since different material were used for the transistor's insulator. The toxe value which is the oxide thickness (t_{ox}) of gate insulator is where it differs between a FinFET and high-k FinFET. The value of toxe used in the model is the equivalent oxide thickness for different materials [7]. Generally, $1.8e^{-9}$ is for SiO_2 gate insulator that is employs for FinFET whereas for high-k FinFET is $1.9e^{-9}$ for HfO_2 gate insulator shown in. The I-V characteristics were obtained from the simulation using LTspice. The common variables of transistor such gate size: height and length will be kept constant. Only the material use for the gate will be changed in order to get a clear picture of the differences in term of gate leakage for both SiO_2 and HfO_2.

III. RESULT AND DISCUSSION

As mentioned previously, the simulation performed is to investigate the effect of high-k on FinFET performance. The comparison was made between n-type MOS and FinFET transistor in 3D model, I-V characteristics and as an inverter. Further simulations were performed to examine the high-k FinFET chain inverter.

Figure 2 and Figure 3 show the differences of a planar transistor compared to a FinFET respectively. The 3D models of both planar and FinFET transistor placed side by side (nMOS at the right side and FinFET at the left side) is shown in Figure 2. Second poly-Si deposition is required in order to make it a FinFET transistor as shown in the figure. Due to the different fabricating method for FinFET, dual doped (n+/p+) of gate insulator by ion implementation is used as gate electrodes [9].

In Figure 3, the marked part shows the gate insulator. That is where it differs from a planar transistor. The planar transistors will have a poly-Si gate insulator whereas high-k FinFET will have HfO_2 gate insulator which is one type of a high-k material that is used for this FinFET. A major distinction between FinFET and planar transistor is a notable narrowed of active region (fin) where it was a modification from a planar complementary metal oxide semiconductor (CMOS) process [9].



Part 1: 3D model of FinFET and nMOS transistor

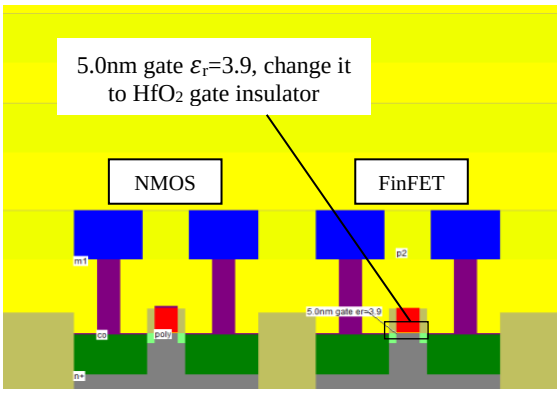
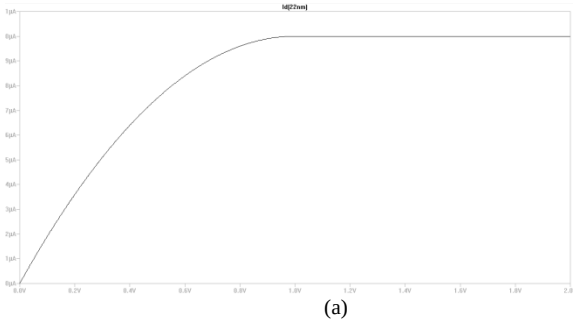


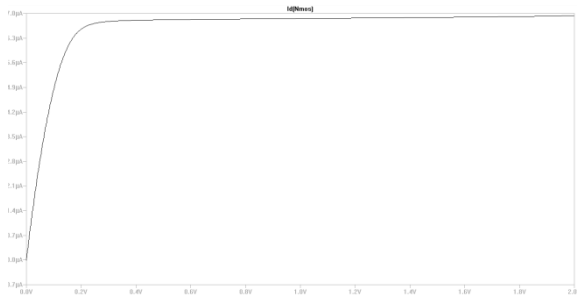
Figure 2: The difference between planar nMOS (left) and FinFET(right)

Figure 3: The cross section of both planar and FinFET transistors

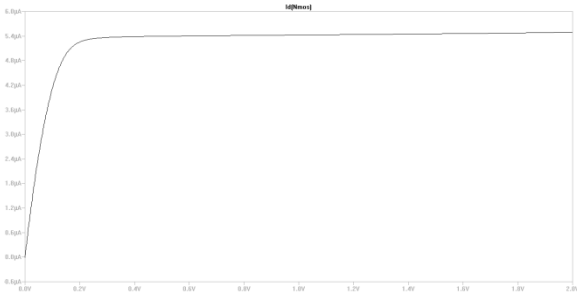
Part 2: I_D-V_D characteristics of planar, FinFET and high-k FinFET transistor



(a)



(b)



(c)

Figure 4: I_D vs. V_D graph of 22nm node technology of (a) planar nMOS, (b) n-type FinFET and (c) n-type high-k FinFET

The results of I-V characteristics were exhibited in Figure 4 where the I_D-V_D graphs were obtained from the SPICE simulation of single n-type transistor with characteristics of a 22nm gate length device with various material of gate insulator.

Figure 4(a) shows the I_D-V_D characteristics of nMOS device with gate length of 22nm. Same characteristics were also plotted for n-type FinFET transistor. A steeper slope for graph in Figure 4(c) when compared to Figure 4(b) shows that the new transistor having the high-k gate insulator FinFET exhibit lower current to operate before it start to saturate. To compare it to planar transistor, it requires more power to operate which will be less productive as the simulation shows very significant difference of I_{ON} required to operate the planar transistor.

As shown in the simulation, FinFETs provide higher I_{ON} than planar transistor, resulting in faster switching times. On the other hand, bulk CMOS has several leakage mechanisms: subthreshold leakage, gate leakage, reverse-biased junction, band-to-band tunneling and gate-induced drain leakage [10]. However, in FinFET, there are two leakage mechanisms: the subthreshold current and gate leakage [11].

Figure 5 indicates a reduction of current required to turn on the transistor. Planar nMOS consumed higher current to turn on the transistor compared to FinFET and high-k FinFET. That would be a drawback factor as it requires high power to operate and lower its performance.

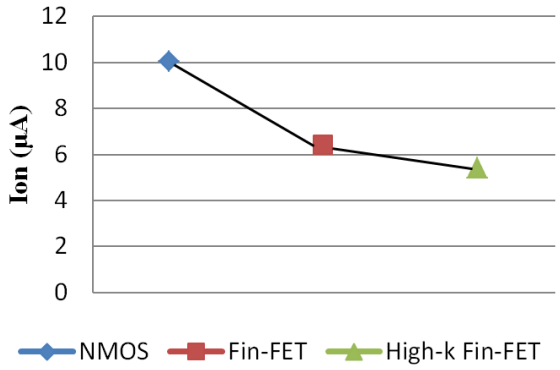
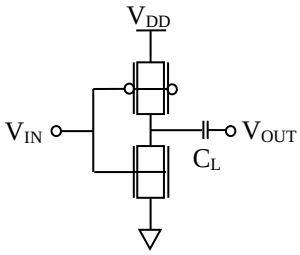


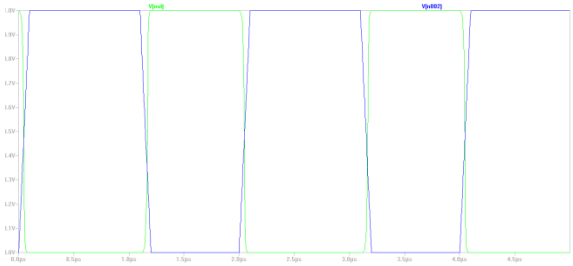
Figure 5: The on current (I_{ON}) for nMOS, FinFET and high-k FinFET

Part 3: Inverter of planar, FinFET and high-k FinFET transistor

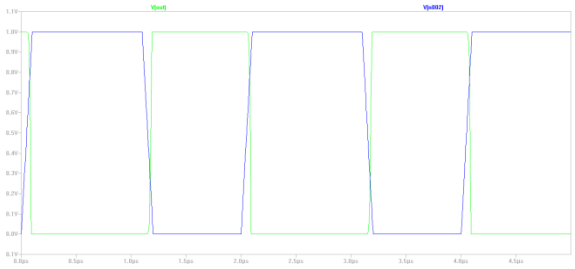


(a)

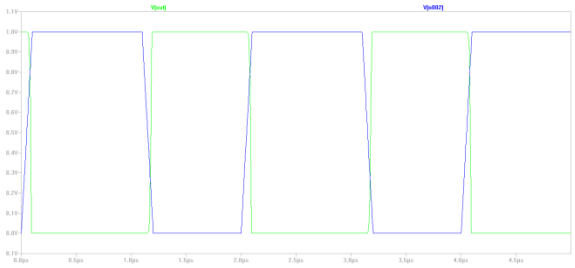
Figure 6(a) shows the schematic of FinFET inverter design where the pull-up transistor is normally a p-type transistor and the pull-down transistor will be the n-type transistor.



(b)



(c)

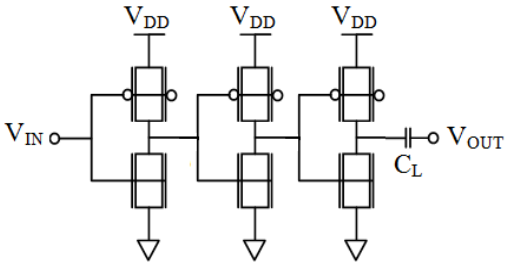


(d)

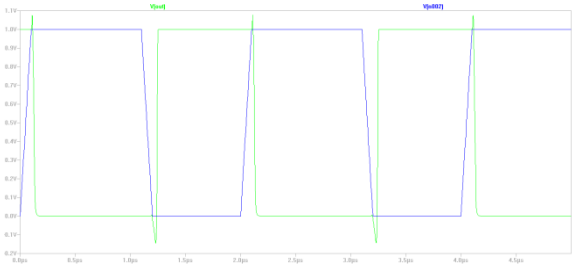
Figure 6: Schematic of inverter (a) and transient input/output characteristics of (b) inverter, (b) FinFET inverter and (d) high-k FinFET inverter

All the SPICE output simulation of the three types of inverter that are being discussed in this paper gives the same output as shown in Figure 6(b), Figure 6(c) and Figure 6(d) which appear to exhibit 1.0V as it is a 1.0V inverter itself. There are no big differences between the transistors as it is only a single transistor.

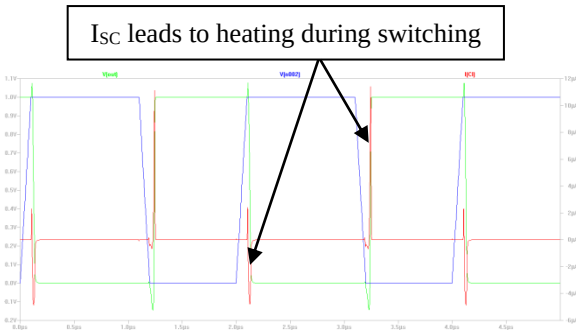
Part 3: High-k FinFET chain inverter



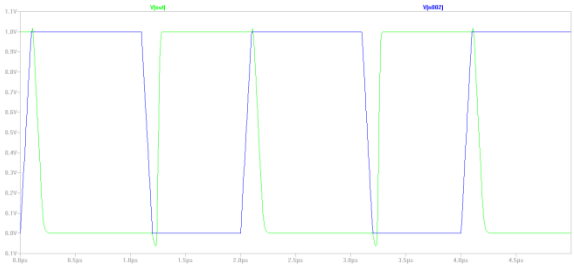
(a)



(b)



(c)



(d)

Figure 7: The (a) schematic of chain inverter [7] and the (b) transient characteristic without I_{SC} effect, C_L=100fF, (c) with I_{CS} effect, C_L=500fF and (d) when using C_L=750fF.

Further simulations were performed for high-k FinFET for chain inverter to analyze the performance. Figure 7(a) shows the schematic of three chain inverters that employ the high-k FinFET. The results of timing diagram were investigated for three different C_L values as tabulated in Table 1.

The glitches formed in Figure 7(b) for the output of inverter are due to two factors which are the capacitor current (I_{CL}) and short circuit current (I_{SC}). But, I_{SC} is more dominant and greatly affect the output of the inverter itself.

The transient characteristic of an inverter and the I_{SC} during the switching operation is shown in Figure 7(c). The short-circuit power dissipation in the inverter is because of the I_{SC} n-type FinFET where it is maximum during the switching process [12]. Thus, raise the problem of heating of the device.

The effects will be greater for a chain inverter compared to just a single inverter as shown in Figure 7(c) and 7(d). This is because the effects of I_{CL} and I_{SC} of the inverters present in the chain configuration will be the total up as it is a series of inverter.

TABLE I DIFFERENCES OF OUTPUT VOLTAGE DUE TO DECREASING LOAD CAPACITANCE

C_L (F)	V_{out}(V)	I_{SC} (µA)
100f	1.075	11.15
500f	1.016	19.18
750f	1.010	20.86

Short circuit current flows during the brief transient when the pull down and pull up devices both conduct at the same time where one (or both) of the devices are in saturation. The load capacitance (C_L) used for the design is kept at smaller value as it is one of the contributing factor that cause an increase in the short circuit current [8]. Table shows a significant loss of output voltage when the C_L is increased. Thus, the time for charging and discharging of C_L would be reduced as a good way of proposing an improvement for the realization of high-performance circuit. Transistor sizing may help to improve performance as long as the delay is dominated by the extrinsic (or load) capacitance of fanout and wiring [9].

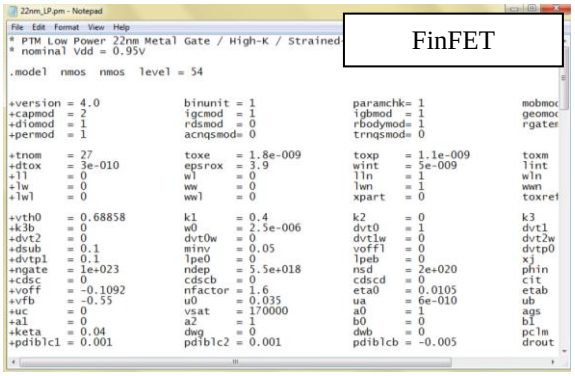
IV. CONCLUSION

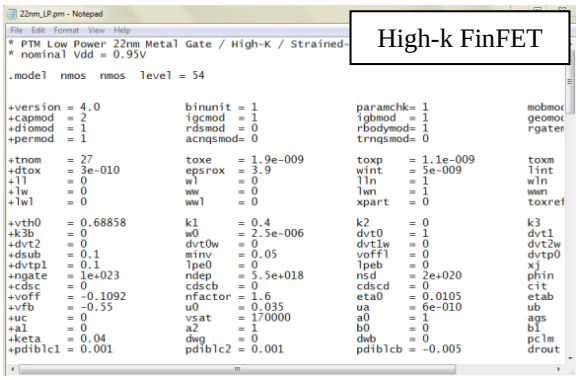
As a conclusion, this paper provides the comparison of FinFET with planar transistor for 22nm technology for both types of transistors. The FinFET device of n-type and chain inverter has been simulated using LTspice and various characteristics are plotted. The investigation is about the different type of transistor structure, material and its performance. The results show that FinFET outperform the planar transistor for the current consumes for switching process of the transistor.

ACKNOWLEDGMENT

The author would like to thank Universiti Teknologi MARA (UiTM) Malaysia, Suhana Sulaiman, PTM (http://ptm.asu.edu/) for the SPICE model and the people from LTspice : LTspice/SwitcherCAD III - Groups - Yahoo! for all the guidance, support and advice provided to me throughout the final year project.

V. APPENDICES





VI. REFERENCES

[1] Chris A. Mack, 2011, "Fifty years of Moore's Law," *Semiconductor Manufacturing, IEEE Transactions on*, vol. 24, no. 2, pp. 202-207, May, 2011.

[2] A. Breed and K.P.Roenker, "Dual-gate (FinFET) and Tri-Gate MOSFETs: Simulation and Design," *Semiconductor Device Research Symp.*, Cincinnati, Ohio, 2003, pp. 150-151.

[3] E.P. Gusev *et. al*., "Advanced high-k dielectric stacks with polySi and metal gates: Recent progress and current challenges," *IBM J. Research Develop.*, vol. 50, pp. 387-410, July 2006.

[4] K. Mistry *et al*., "A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging", *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, Washington, DC, 2007, pp. 247-250.

[5] P. Bai *et al*., "A 65nm Logic Technology Featuring 35nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD, and 0.57um^2 SAM Cell," *IEDM Tech. Dig.*, pp. 657-660, 2004.

[6] P. Wambacq, "Analog and RF Circuits in 45nm CMOS and Below: Planar Bulk Versus Finfet," *Solid-State Circuits Conf., 2006. ESSCIRC 2006. Proc. of the 32nd European*, Montreux, Switzerland, 2006, pp. 54-57.

[7] S. S. Rathod *et al*., "Rad-Hard 32 nm FinFET Based Inverters," *India Conference (INDICON) 2009 Annual IEEE*, Gujarat, 2009, pp. 1-4.

[8] Chenming C. Hu, "Modern Semiconductor Devices for Integrated Circuits" 1st ed., Prentice Hall, 2009, ch.5, pp. 67.

[9] Chenming C. Hu, “Modern Semiconductor Devices for Integrated Circuits” 1st ed., Prentice Hall, 2009, ch.5, pp. 191.
[10] Bin Yu *et al*., “FinFET Scaling to 10nm Gate Length,” *Int. Electron Devices Meeting 2002. IEDM '02*, California, USA, 2002, pp. 251-254.
[11] S. Mukhopadhyay *et al*., “Accurate Estimation of Total Leakage Current in Scaled CMOS Logic Circuits Based on Compact Current Modeling,” *Proc. Design Automation Conf*, 2003, pp. 169–74.
[12] H. Ananthan *et al*., “FinFET SRAM – Device and Circuit Design Considerations,” In *Int.Symp.on Quality Electronic Design*, 2004, pp 511–6.
[13] V. Narendar *et al*., “Design of High-performance Digital Logic Circuits based on FinFET Technology,” *Int. Journal of Computer Applications* 41(20), New York, USA, 2012, pp. 40-44.