8-BIT SUCCESSIVE APPROXIMATION REGISTER (SAR) ANALOG TO DIGITAL (ADC) LOGIC DESIGN

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***Abstract* – A 8-bit SAR logic of SAR ADC has been realized in a HP 0.5µm SCN3M Complementary Metal Oxide Semiconductor (CMOS) process. The power consumption is 3.59mW with resolution of 8-bit. The speed is 125KHz with the supply voltage of 5V. The SAR logic has been designed in custom design approach.**

***Keyword*: Successive approximation register (SAR) Analog to digital converter (ADC), SAR logic, power consumption, CMOS, resolution.**

1. INTRODUCTION

The successive approximation register analog to digital (SAR ADC) is one of the most widely used types of ADC compared with other ADC architecture. SAR ADC provides number of advantages [4]. First, low power consumption because only one comparator in the whole system. Second, high resolution and accuracy can be achieved using capacitor array during data conversion. Third, has more complex circuitry than digital-ramp ADC but shorter conversion time. In addition, SAR ADC has a fixed value of conversion time.

In this paper, development of 8-bit SAR ADC digital control logic is presented.

1.1 SAR ADC Architecture

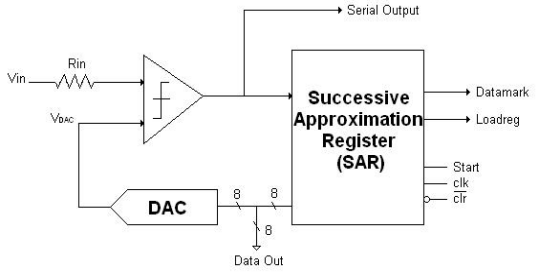

Figure 1: SAR ADC Block Diagram

The block diagram of Successive Approximation Register (SAR) Analog-to-Digital (ADC) is shown in Figure 1. The SAR ADC consists of three modules, which are comparator, SAR control logic and Digital-to-Analog Converter (DAC). The implementation progresses of the SAR like a binary search algorithm to arrive at the final digital output with an error of no more than $0.5V_{LSB}$ [3].

At starting of a conversion, all the bits of SAR are reset to "0" except the MSB which is set to "1". The SAR output drives the internal DAC. If the DAC output is greater than the analog input, this bit in the SAR is reset, otherwise it is left set. The process is repeated with each bit in turn. When all the bits have been set, tested, and reset or not as appropriate, the contents of the SAR correspond to the value of the analog input, and the conversion is complete. The end of conversion is indicated by a loadreg which means that the data will be loaded to register. An N-bit conversion takes N steps.

2. SAR LOGIC DESIGN

2.1. Block Diagram of SAR Logic

The successive approximation logic is based on the shift register and register. Figure 2 shows the block diagram of the SAR logic. SAR logic consists of 10 bit shift register, register low to high and code register.

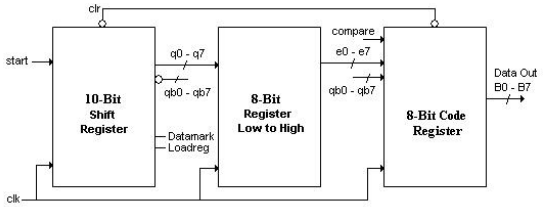

Figure 2: Block Diagram of SAR Logic

2.2. Shift Register

A shift registers are used to store information in the register one bit at a time. The type of shift register is serial in/parallel out and acts on the stored information in a register by shifting its contents to the right. The block diagram of shift register is shown in Figure 3.

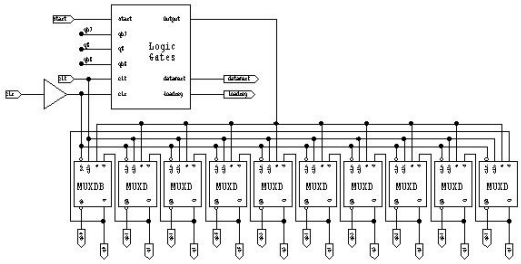

Figure 3: 10-Bit Shift Register

The block diagram consists of control logic gates (Appendix B) and shift register. The internal structure of shift register consists of 2 to 1 multiplexer and D flip-flop. On the last register (10th register) has an inverter in the structure as shown in Figure 4. The inverter will converted the input bit from 0 to 1 or otherwise. The timing diagram of shift register is illustrated in Figure 5. The first state, S12, is used to clear all bit at the register. At state 11, datamark will be set which means a start of a conversion. Sampling occurs at state 10 and the 10th register (q9) will be set. States 9 to 1 are bit shifting states where bits 8 through 1 are determined in parallel. The 8 bit code is ready during state 12 of the next conversion cycle and so that loadreg will be set.

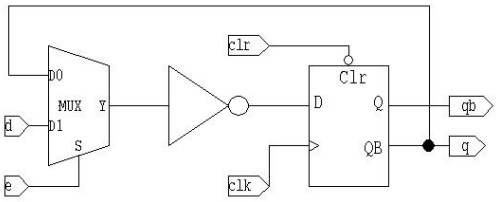

Figure 4: Structure of shift register with inverter.

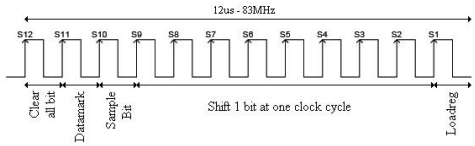

Figure 5: Timing diagram for operation of shift register

2.3. Register Low to High

A register is a temporary storage device. The type of register used is parallel register. The contents of the register are called a WORD. For an 8 bit register is an 8-bit word. The schematic circuit of 1-bit register low-to-high is shown in Figure 6 and 8-bit register in Figure 7. This circuit will receive data and transfer it at the proper time. It is also improved the signal flows through it from low signal to the high signal. Truth table for the operation of register is shown in Table 1.

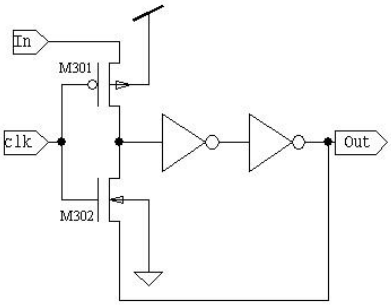

Figure 6: 1-Bit Register Low-to-High

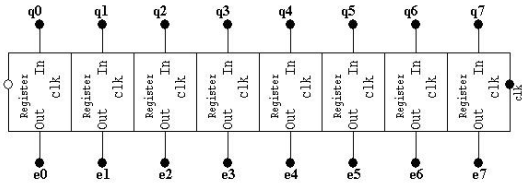

Figure 7: 8-Bit Register Low-to-High

Table 1: Truth Table for Register low-to-high

Clock	PMOS	NMOS	Out
Rising	OFF	ON	Stay
Falling	ON	OFF	In

2.4. Code Register

The implementation of code register is illustrated in Figure 8. It is consists of register and NAND gate. NAND gate used to improve the conversion time. The internal structure of a register is shown in Figure 9. It is composed by a D Flip-flop with a multiplexer (MUX). MUX will control which one of the two data input, D0 and D1 will be transmitted to the output. D0 and D1 are selected from the output of previous flip-flops stage and the output from the comparator respectively. Truth table for flip-flop outputs is shown in Table 2.

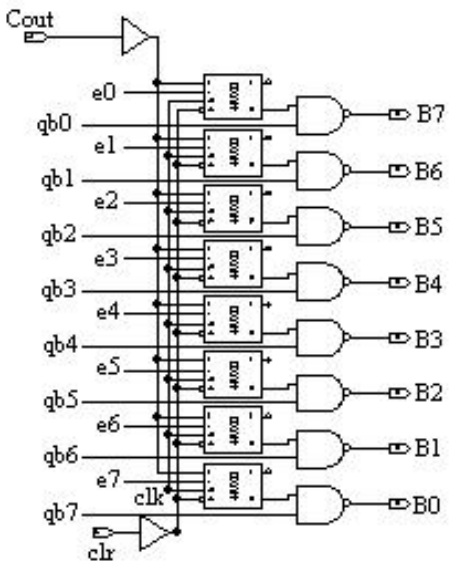

Figure 8: 8-Bit code register

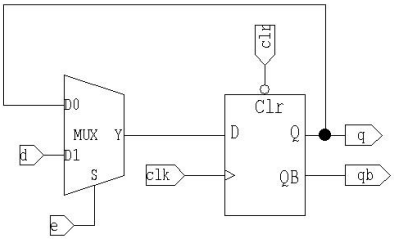

Figure 9: Structure of shift register

Table 2: Truth Table for Flip-Flop output

Select, *s*	Operation
1	Comparator output, *D1*
0	Memorize present stage, *D0*

3. RESULTS AND DISCUSSION

The 8-bit SAR ADC logic was designed in a HP 0.5µm SCN3M technology. The SAR logic was evaluated in terms of power consumption, resolution and speed. The whole structure of the schematic is shown in Figure 10 and the internal structure of register in Figure 11.

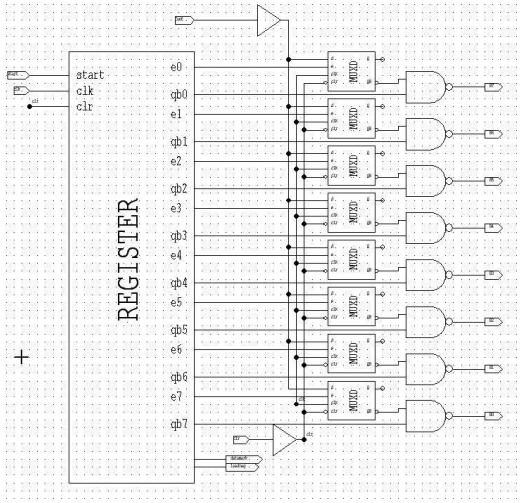

Figure 10: Structure of SAR Logic

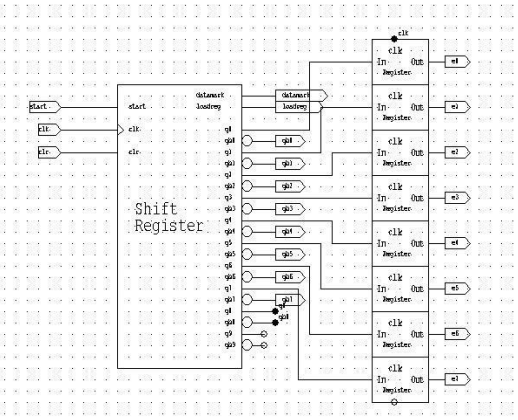

Figure 11: Structure in module of register

3.1 Shift Register Characteristics

The type of shift register is serial in/parallel out or SIPO shift register and shift in right direction. The waveform of shift register is shown in Figure 12.

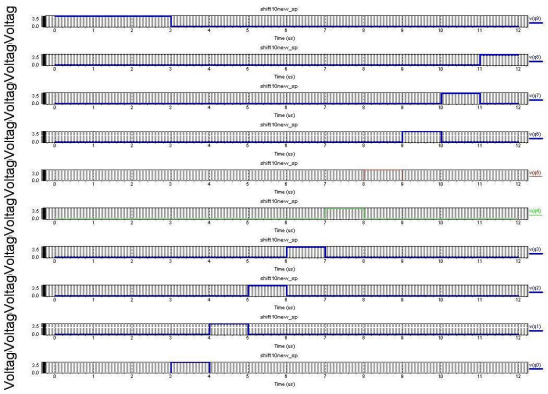

Figure 12: Output waveform of shift register

The propagation delay of shift register is 1µs. This delay is mentioned in term of clock cycle time. The risetime and falltime was found when the shift register run at the voltage of 1V which is 14.84ns and 6.11ns respectively. The power consumption for the shift register is 3.06mW.

3.2 Register Low to High Characteristics

Figure 13 shows the output waveform of register. The input of the register is actually combined from the output of shift register before. It shows that time taken for a bit stored in the register is 0.5µs and a bit stay high until the falling edge of the clock. The propagation delay is also same with the shift register where 1µs delay and the power consumption included of shift register is 2.78mW.

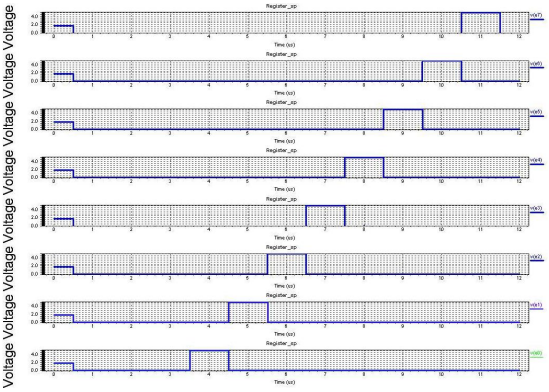

Figure 13: Output waveform of register

3.3 Code Register Characteristics

The output waveform of code register is mentioned in Figure 14. The code register is used as a storage register where it stored the data from comparison output from the comparator. The specification of code register is mentioned in SAR Logic characteristics.

3.4 SAR Logic Characteristics

The SAR logic was implemented in terms of resolution, power consumption and conversion speed. The resolution of this project is 8-bit and to find the resolution for 1 step is shown below.

$$Step\ Size = \frac{Max.\ Rated\ Output\ Voltage}{2^n}$$

$$= \frac{5}{2^8} \quad = \frac{5}{256}$$

$$= 19mV$$

The resolution of 1 step size for 8-bit SAR logic is 19mW.
For a 8-bit SAR, the maximum conversion time is always 8 clock periods or

$$1\ clock\ \ period = 1\,\mu s \quad so\ that$$

$$8 \times\ 1\,\mu s = 8\,\mu s$$

From conversion time, the speed was initialized which is 125KHz.
The power consumption was found from the netlist output after the simulation was completed. For the project, the power consumption is 3.59mW at the supply voltage of 5V. The output waveform of 8-bit SAR logic is shown in Figure 14. From the figure, the digital output code is 10010011_{10} or 147_2. The conversion completes the conversion at 8 clock cycles in 8µs and loadreg was set HIGH indicating that the conversion is complete and data are ready.

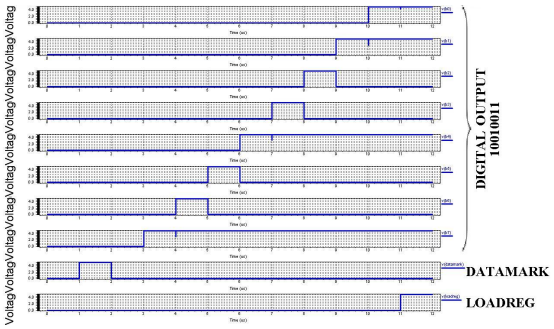

Figure 14: Output waveform of 8-bit SAR logic

3.5 Comparison

The transistor sizing in the project was assumed in the different value of width. According to the MOSIS HP 0.5µm SCN3M SCMOS design rule, the minimum width of the MOSFETs in analog application is 5λ to have optimum performance [7]. The comparison between the difference size of width and power consumption was shown in Figure 15. Appendix A shows the difference size of width in each schematic of SAR logic.

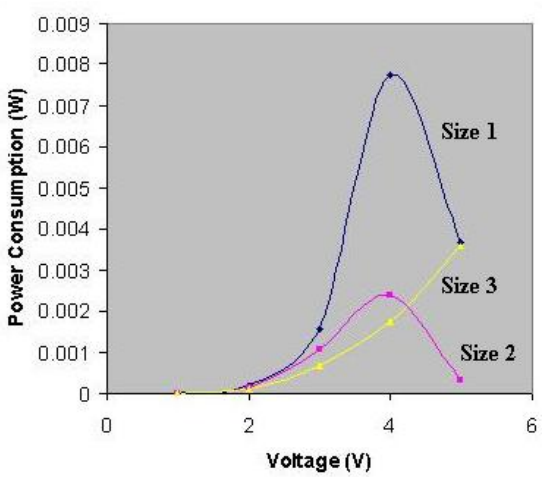

Figure 15: Graph power consumption over voltage supply in 3 different size of width.

From Figure 15, it shows the three size of width. Size 3 was represented in the project. From voltage 0V to 4V, all graphs were increased and showed that Size 3 has a lower power consumption but when reached at 5V, graph of size 1 and 2 were decreased instantaneously except graph of size 3. It means that the power consumption of size 3 is stabilized in performance.

4. CONCLUSION

This paper presents an 8-bit SAR ADC logic which designed in a HP 0.5µm CMOS technology. To complete one conversion, 9 clock cycles are needed. To summarize the performance, the conversion time is 8µs for the 8 clock periods with the speed of 125KHz. It was concluded that the conversion time has fixed value in SAR ADC. The power consumption is as low as 3.59mW and the resolution of 8 bits are achieved.

4.1 Future Development

The power consumption of the successive approximation register can be improved by sizing the transistor size and logical effort of the architecture. The block of comparator and DAC will be developed with lower power consumption to complete the whole structure of SAR ADC. The conversion time can be further reduced by a number of ingenious techniques, such as comparator speed-up techniques, or variable-clock techniques, which exploit the faster settling times in the least-significant bit positions.

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REFERENCE

[1] Ronald J. Tocci, Neal S. Widmer, "DIGITAL SYSTEMS Principles and Applications", Prentice Hall, Eighth edition, 2001.

[2] Daniel D. Gajski, "Principles of Digital Design", Prentice-Hall, International edition, 1997.

[3] Hassan A. Farhat, "Digital Design and Computer Organization", CRC PRESS, 2004.

[4] Chih-Kai Kang, Jia-Yi Chen, Juang-Ying Chueh, "A 10-bit 10MHz Samples/s 5mW Successive approximation Register A/D converter".

[5] Tzu-Hen Hsu, Ying-Shun Chuang, Chun-Ping Huang,"A 10-bit 40MS/s Successive Approximation Register A/D Converter".

[6] Donald P. Leach, Albert Paul Malvino,"DIGITAL PRINCIPLES & APPLICATIONS", Fifth edition, GLENCOE McGraw-Hill, 1995.

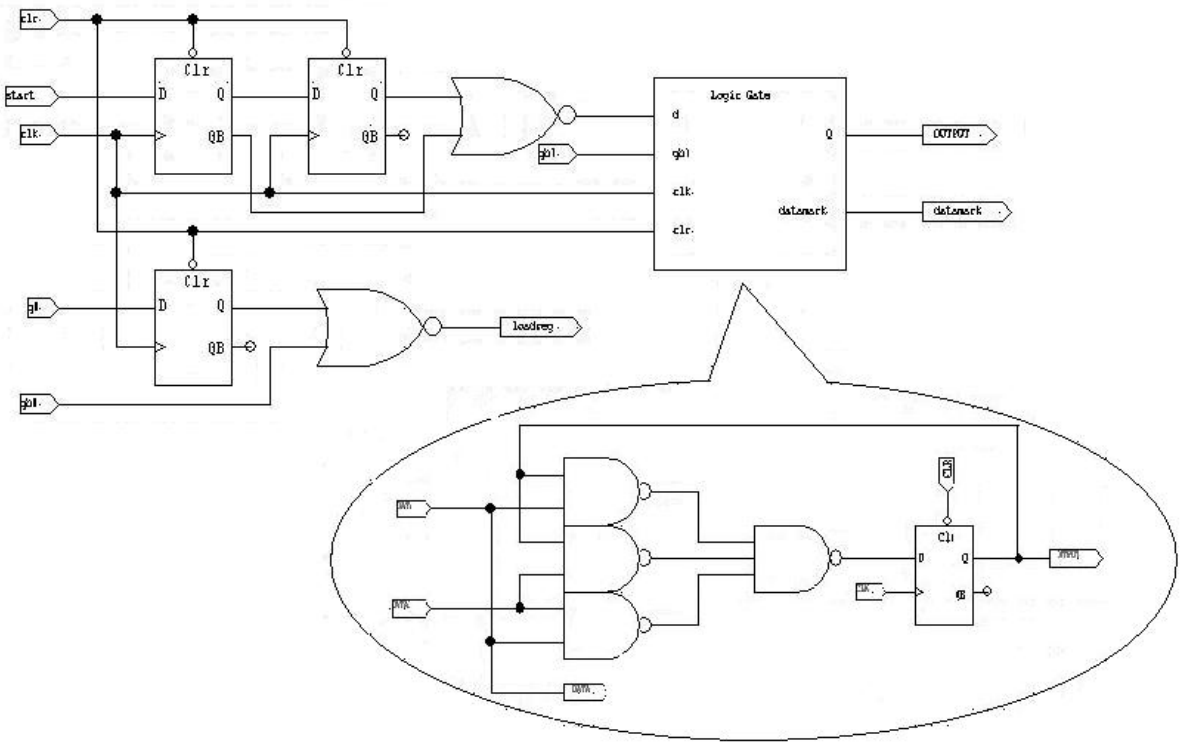
[7] MOSIS Integrated Circuit Fabrication Service, In website of www.mosis.org

APPENDIX A

	Size of Width (λ)		
Transistors	Size 1	Size 2	Size 3
BUFFER			
M1,M2	18	10	10
M3,M4	28	20	15
DFF			
M7,M8,M11,M12 M20,M21,M24 M12,M17,M16	15	10	10
M26,M29,M27	22	15	15
M1,M2,M3,M4	6	5	5
M5,M6	17	15	10
M9,M10	14	10	10
M18,M19,M23	16	15	10
M22,M25	24	20	15
M14	9	5	5
M28	27	20	15
M15	11	10	5
MUX			
M11,M12 M6,M7,M8,M9,M10	28	20	15
M1,M2,M3,M4,M5	21	15	10
NAND3/NAND2/NOR2/INV			
M1,M2,M3,M4,M5,M6	28	20	15
REGISTER			
M301,M302	6	6	5

* Size of length (L) is all same for the transistors which are 2λ

APPENDIX B


clr
start
clk
Clr
D
Q
QB
Logic Gate
d
Q
clk
clr
datamark
loadreg