Investigation of Si_3N_4 Capping Layer and Embedded SiGe Effect on 90 nm CMOS Devices

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***Abstract* – This paper highlights the effect of Si_3N_4 capping layer, embedded SiGe in the source/drain and SiGe layer on the bottom of the strained silicon for strained-silicon technology effect on 90 nm Complementary Metal Oxide Semiconductor (CMOS) performance focusing on threshold voltage and drain current parameters. Strained silicon is used to increase saturated NMOS and PMOS drive currents and enhance electron mobility. Compressive strain is introduced by two techniques strained in the PMOS channel using SiGe such as uniaxial strained and biaxial strained. Tensile strain is introduced in the NMOS channels by using a post silicon-nitride capping layer. ATHENA and ATLAS simulators were used to simulate the fabrication process and to characterize the electrical properties respectively. It can be concluded that NMOS strained technology having high tensile stress improve by 46.9% drain current. PMOS strained technology having compressive stress using biaxial strained PMOS improve 16.4% while uniaxial strained PMOS improve 21.4%. The strained technology were the best on 90 nm for CMOS device is combination of Si_3N_4 film tensile strain for NMOS and uniaxial compressive strain for PMOS.**

***Index Terms* – Strained silicon, Compressive strain, Tensile strain, Nitride (Si_3N_4) capping layer, Silicon Germanium (SiGe).**

I. INTRODUCTION

STRAINED-SILICON (Si) using a novel low cost process flow is introduced. Unlike the traditional approach where biaxial strain is applied into the channel from the bottom using strained-Si on relaxed $Si_{1-x}Ge_x$ [1], and uniaxial strain is introduced from the side using (p-type CMOS) and a nitride-capping film with a large tensile stress (n-type CMOS). Transmission electron micrographs (TEMs) of MOSFETs are shown in Fig. 1. Strained-Si mobility enhancement is well-known and has found many applications in mechanical sensors. However, until recently [2], there has been no published literature on incorporating either biaxial or uniaxial strained-Si into a commercial CMOS microprocessor logic technology. In this letter, we describe the strained-Si process flow used in a 90-nm logic technology. We focus only on the hole mobility enhancement with strain since the conduction band splitting and mobility enhancement with a tensile nitride-capping layer [3].

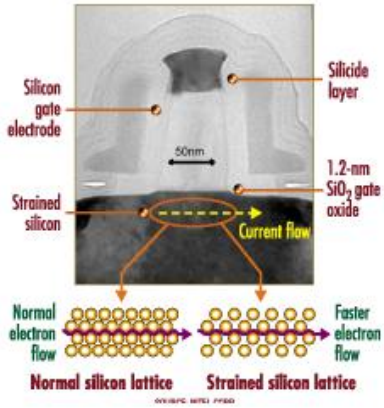


Fig.1 TEM of 50 nm MOSFET

Several techniques are used to introduce strained silicon in the device. Most of these techniques involve the epitaxial growth of one or more silicon layers on top of one or more layers of $Si_{1-x}Ge_x$. The lattice mismatch between the silicon layers and $Si_{1-x}Ge_x$ layers induces strain and corresponding stress in these structures. A common technique is to grow strained silicon on relaxed $Si_{1-x}Ge_x$ [4][5].

However, this method introduces a lower bandgap material ($Si_{1-x}Ge_x$) into the body of the MOSFET, which requires additional care to avoid punch-through. A different approach is to introduce $Si_{1-x}Ge_x$ pockets into the source and drain of the PMOS device. These pockets create compressive stresses in the channel area. The NMOS device was fabricated using a standard NMOS process flow but, at the end of the process flow, a highly tensile silicon-nitride cap layer was

deposited, which covered the source, drain, and gate stack. This layer created tensile stresses in the channel. In both of the abovementioned cases, stresses improved the performance of the transistor.

For strained Si technology there are two major approaches of applying strain to the channels: Silicon Nitride (Si_3N_4) film and Silicon Germanium (SiGe). In this paper, several technology had been covered which are Si_3N_4 capping layer and SiGe.

A. Silicon Nitride (Si_3N_4) Capping Layer

Silicon nitride (Si_3N_4) capping layer produce a high level of strain. Si_3N_4 film can have either tensile or compressive strain depending on the deposition technique. The Si_3N_4 film strain can be effectively applied to the channel. Because of this, the effectiveness of the approach remains untouched even as geometry shrinks. It can apply tensile strain to increase electron mobility in NMOS transistor channels, and compression strain to increase hole mobility in PMOS transistors as shown in figure 2.

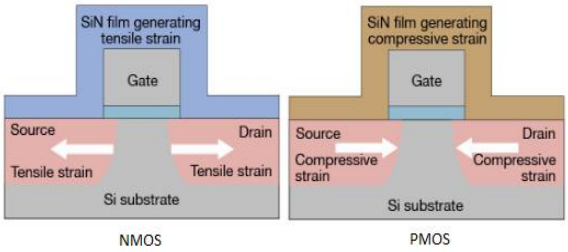


Fig. 2 : The Si_3N_4 film strain can applied in NMOS and PMOS transistor.

The tensile capping layer deposited by thermal chemical vapor deposition (CVD) can improve the performance of NMOS due to the induced tensile strain in the channel region while the compressive capping layer deposited by plasma enhanced CVD can improve the PMOS due to the induced compressive strain in the channel region. Si_3N_4 capping layer with high tensile strained can improve NMOS performance but degrade PMOS performance[6].

The device current will improve up to 25% by increasing the thickness of tensile Si_3N_4 layer. However, the thickness of Si_3N_4 become saturated at 100 nm thick and I_{dsat} gain is also limited. Furthermore, thicker Si_3N_4 capping film causes wafer bending causes wafer crash in process instruments and disables the focus control for photo steppers. And it also degrades the PMOS drive current[7].

B. Silicon Germanium (SiGe)

SiGe is only being used as a method of applying compressive strain to channels in PMOS transistors. There are mainly two techniques of strained PMOS being explored which is shown in figure 3. The main difference is the structure which is for uniaxial strained PMOS can be induced by using SiGe material in source and drain, while for the biaxial strained PMOS has a layer of $Si_{1-x}Ge_x$ deposited at the bottom of strained silicon layer to perform the strained effect.

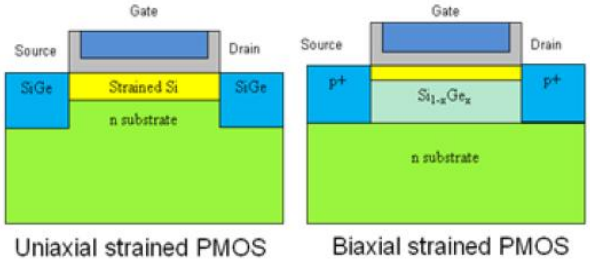


Fig. 3:Two main types of strained PMOS

Uniaxial strained PMOS can be induced by implants SiGe into both source and drain regions to apply strain to the channel. Because the source and drain regions must be made thinner as the design rule is reduced, the SiGe regions must also be made thinner. The only way to maintain the level of strain needed for the channel is to increase Ge concentration.

II. METHODOLOGY

The design process and device modeling for this research was done by using TCAD SILVACO software. The structures of the simulation were simulated from ATHENA window, while the characteristic of the structures was simulated from ATLAS.

A. ATHENA and ATLAS Simulation

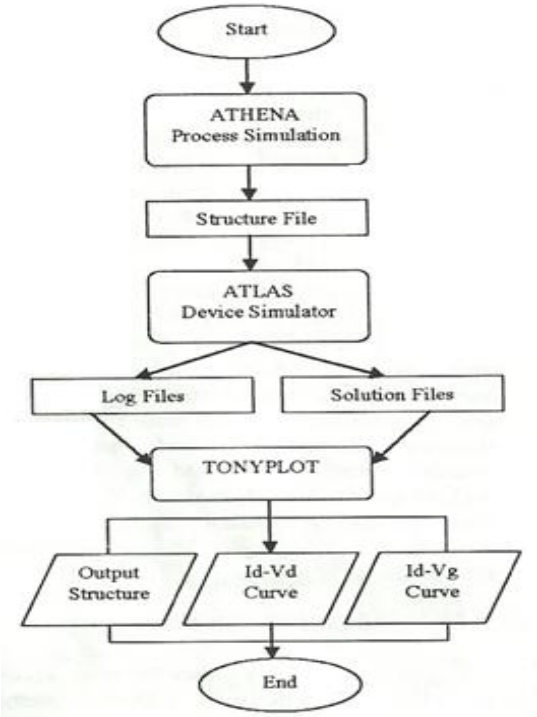


Fig. 4: Modeling flow chart

ATHENA is a process to develop and optimize semiconductor. ATHENA process simulators are used in creating CMOS device structure.

The recipe is simulated and the variable such as temperature, time and material are varied in order to get threshold voltage and other parameters in acceptable range and the structure of NMOS and PMOS. The device structure can be view using Tonyplot. The processes that involve in fabrication are layer deposition, lithography, etching, implantation, oxidation and diffusion.

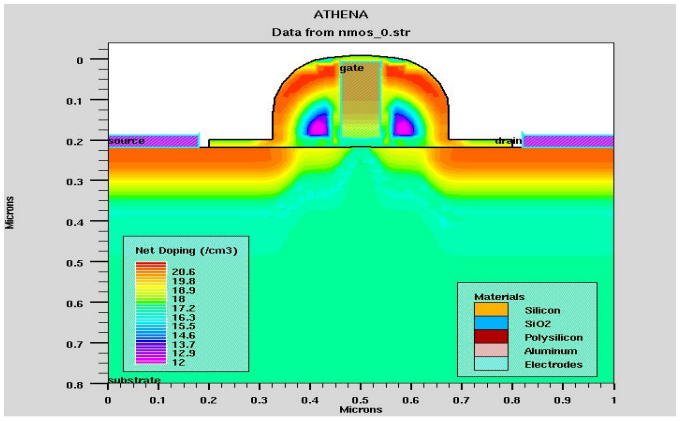
ATLAS is a physical-based two dimensional device simulator. It predicts the electrical behavior of specified semiconductor structure and provides insight into the internal physical mechanisms associated with device operation. ATLAS will simulate the electrical characteristics of the CMOS structure that was created by ATHENA. ATLAS generates I_d-V_d curve, I_d-V_g curve and hence producing threshold voltage (V_t) and drain current (I_d). Figure 4 show the flow of the simulation.

III. RESULTS AND DISCUSSION

Figure 5 shows the cross section of 90 nm NMOS and PMOS. Figure 6 and 7 show the electrical characteristic curve of 90 nm for NMOS and PMOS. Figure 6 is Id-Vd curve for NMOS and PMOS where the voltage gate is set to 1V, 2V and 3V. The drain current for NMOS and PMOS at gate voltage 3V are 0.167 mA and -0.618 mA. Figure 7 is shows the Id-Vg curve for NMOS and PMOS where the drain voltage is set to 0.1V. From the figure 7, ones can determine the threshold voltage value. The drain current and the threshold voltage value can be calculated using equation (1) and (2) respectively.

$$Idsat = \frac{WCox\mu}{L}\left[\left(Vgs - Vt - \frac{Vdsat}{2}\right)Vdsat\right] \quad (1)$$

$$Vt = Vgs(0) - \frac{Vds}{2} \quad (2)$$



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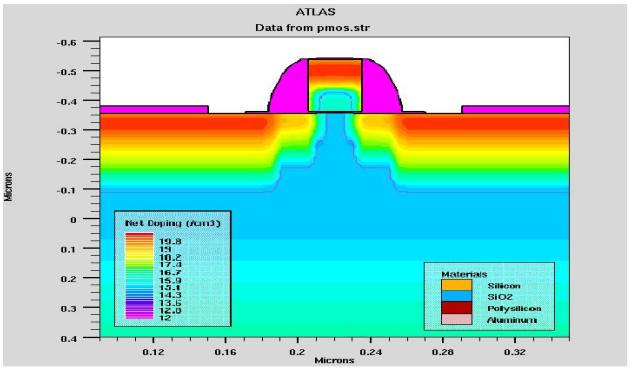
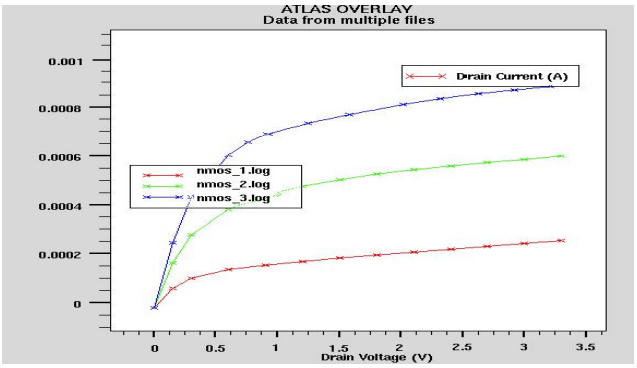


(b)

Fig. 5: Cross section of 90 nm (a) NMOS (b) PMOS



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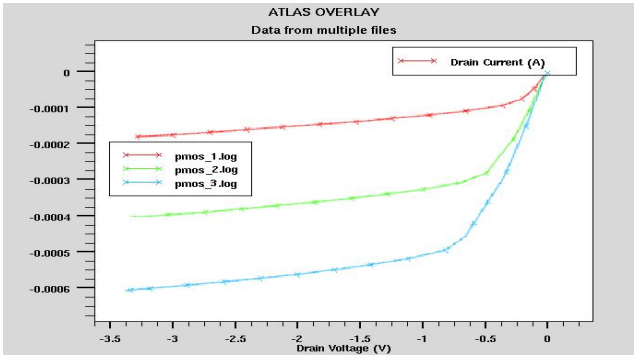

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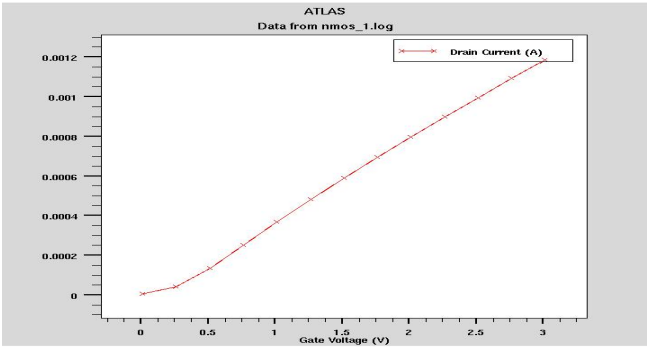
Fig. 6: Id-Vd curve (a) NMOS (b) PMOS



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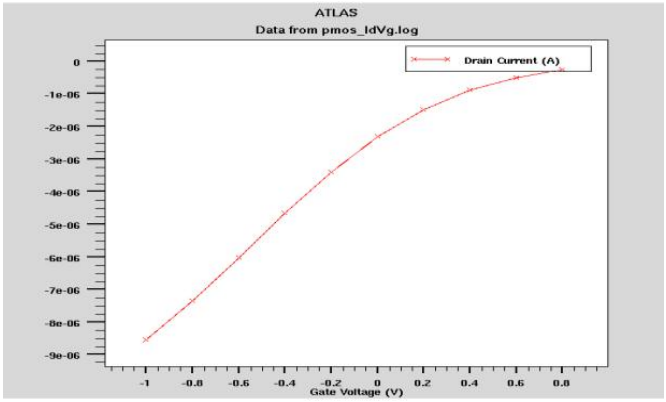


(b)

Fig. 7: Id-Vg curve (a) NMOS (b) PMOS

Table 1 shows the electrical characteristic of NMOS and PMOS for gate length of 90 nm.

TABLE 1
THE ELECTRICAL CHARACTERISTIC OF CMOS FOR GATE LENGTH OF 90 NM

Electrical characteristics	NMOS	PMOS
Vt (V)	0.167	-0.119
Id (mA)	0.843	-0.618

A. Electrical Characteristic of 90 nm CMOS Between Different Strained Technology Techniques.

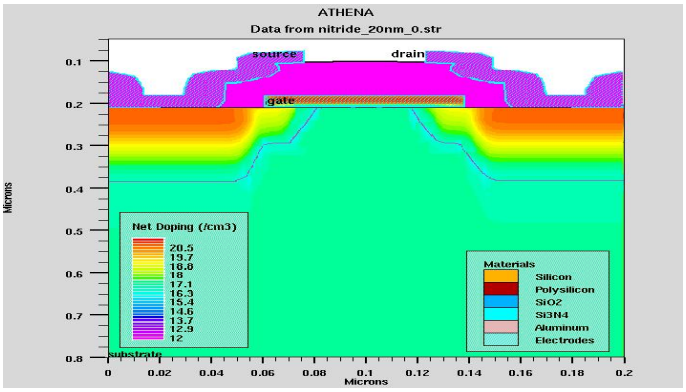
The result of electrical characteristic of the strained-silicon NMOS and PMOS devices with a 90 nm gate length between different strain technology techniques by using silicon-nitride capping layer and silicon germanium. Equation (3) shows the comparison between with and without strained technology focusing on drain current characteristic.

$$\text{Variation of drain current} = \frac{Id\ \text{with strained} - Id\ \text{without strained}}{Id\ \text{with strained}} \times 100\% \quad (3)$$

i. Silicon Nitride (Si_3N_4) Capping Layer

Figure 8 shows the cross section of 90 nm NMOS and PMOS with Si_3N_4 capping layer. Figure 9 shows electrical characteristic curve for Id-Vg curve of 90 nm for NMOS and PMOS with Si_3N_4 capping layer.

Table 2 shows electrical characteristic of NMOS and PMOS with different thickness of Si_3N_4 capping layer. For this research, 20 nm and 80 nm thick of Si_3N_4 capping layer were used to compare the electrical characteristic performance.



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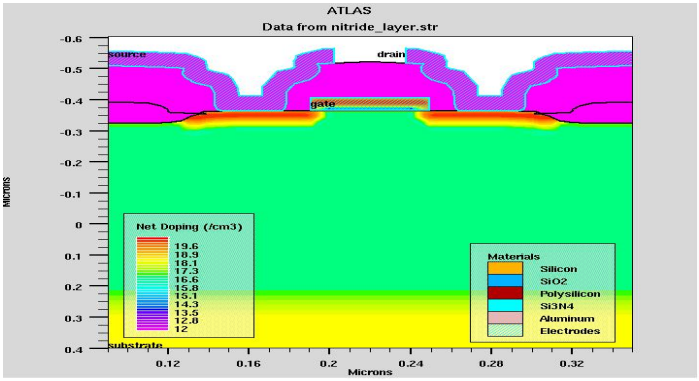

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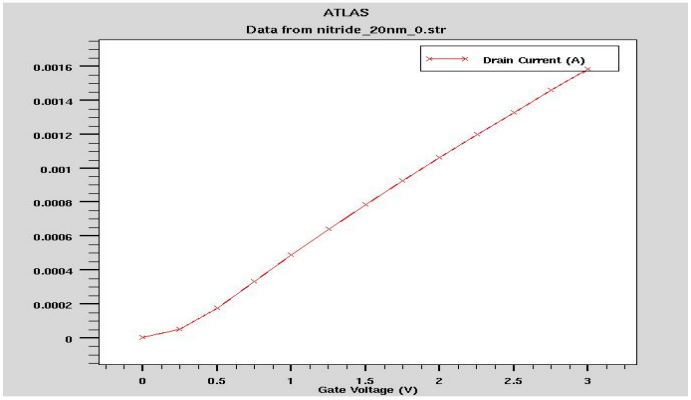
Fig. 8: Cross section of 90 nm with Si_3N_4 capping layer (a) NMOS (b) PMOS



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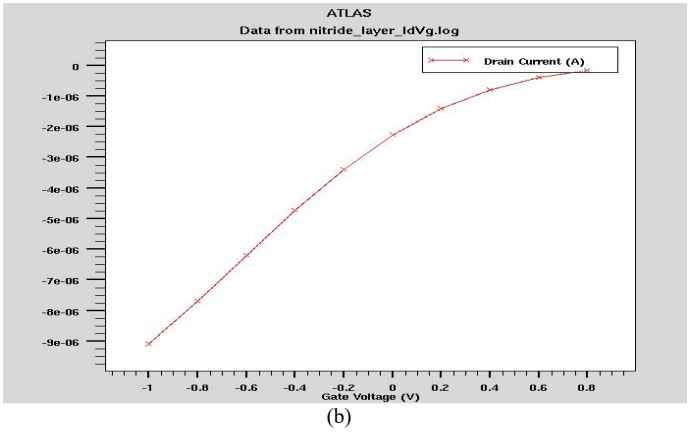

(b)

Fig. 9: Id-Vg curve of 90 nm with Si_3N_4 capping layer (a) NMOS (b) PMOS

TABLE 2

ELECTRICAL CHARACTERISTIC WITH Si_3N_4 CAPPING LAYER

	Silicon nitride thickness	*Vt (V)*	*Id (mA)*
NMOS	20 nm	0.168	1.59
	80 nm	0.167	1.58
PMOS	20 nm	-0.117	-0.633
	80 nm	-0.117	-0.632

From table 2, it shows that CMOS device with the changes of the thickness of Si_3N_4 capping layer has no significant effect on electrical characteristic. For NMOS with 20 nm Si_3N_4 capping layer thick the I_d is 1.59 mA while for 80 nm Si_3N_4 capping layer the current is only 1.58 mA. For PMOS with 20 nm Si_3N_4 capping layer thick the I_d is -0.633 mA while for 80 nm Si_3N_4 capping layer the current is -0.632 mA. In addition, I_d for NMOS and PMOS with different thickness of Si_3N_4 capping layer there are no changes of current reported. Si_3N_4 capping layer cannot be too thick because it can cause wafer bending and thus will cause wafer broken[9].

The electrical characteristics of CMOS with Si_3N_4 capping layer were compared to the electrical characteristic without Si_3N_4 capping layer. Figure 10 shows comparison of 90 nm NMOS and PMOS with and without Si_3N_4 capping layer.

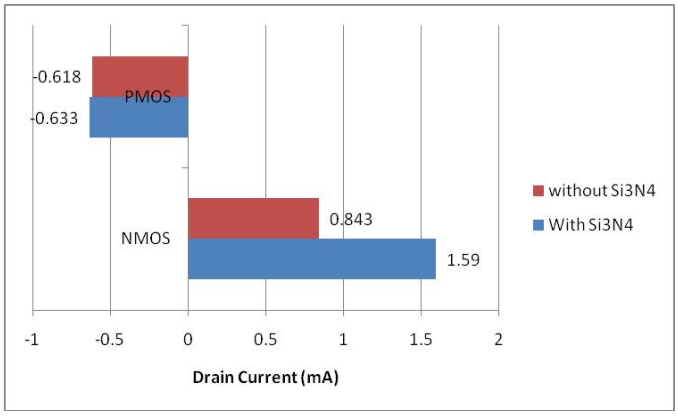

Fig. 10: Drain current comparison of NMOS and PMOS between with and without Si_3N_4 capping layer.

From figure 10, it shows that CMOS with strained technology having higher I_d. Drain current for both NMOS and PMOS were improve. NMOS improve 46.9% while PMOS increase 2.4%. For strained technology, it shows that Si_3N_4 capping layer improve NMOS performance than PMOS performance. It can be concluded that NMOS strained technology having high tensile stress and PMOS strained technology having compressive stress[9]. Thus, Si_3N_4 capping layer strain can be effectively applied to the NMOS device[9].

ii. Silicon Germanium (SiGe)

Figure 11 shows cross section of 90 nm PMOS with biaxial strained PMOS. Figure 12 shows the electrical characteristic curve of 90 nm for PMOS with biaxial strained and uniaxial strained.

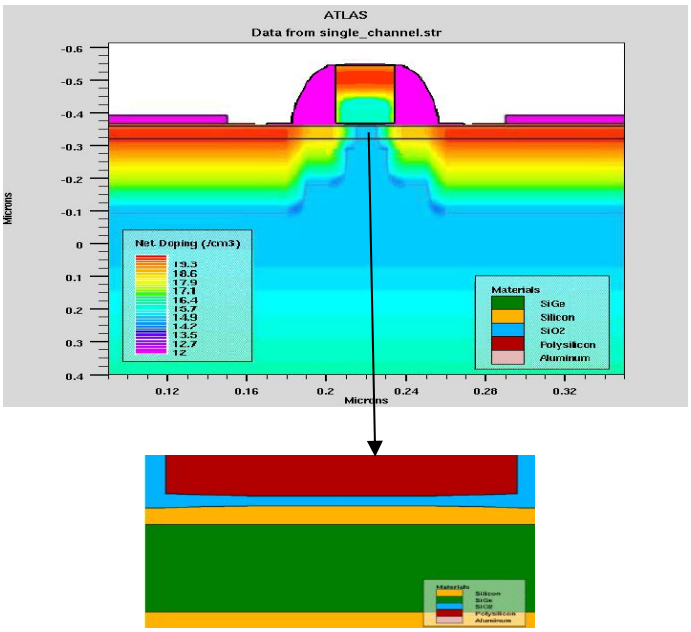

Fig. 11: Cross section of 90 nm for PMOS biaxial strained

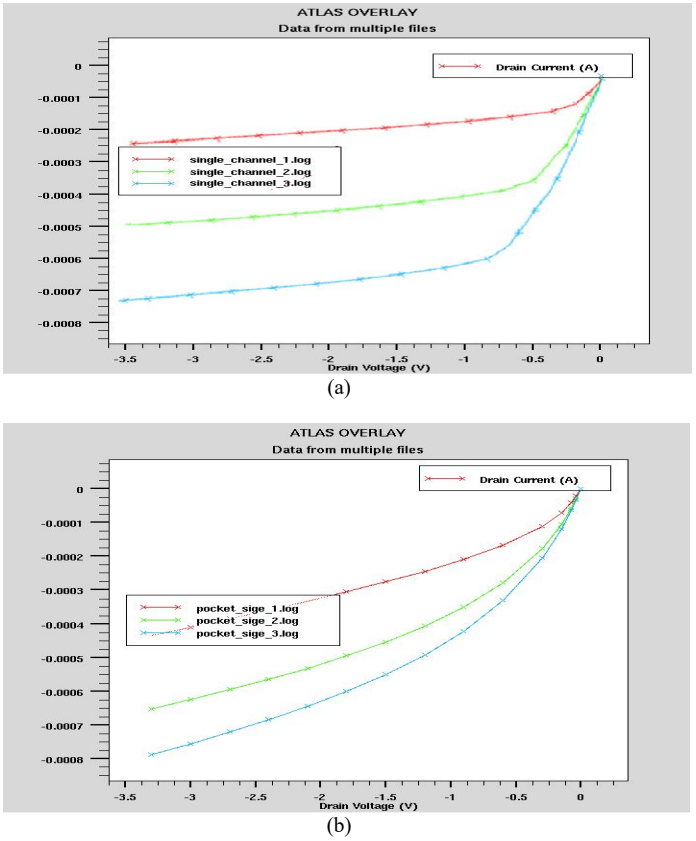

Fig. 12: I_d-V_d curve for PMOS (a) biaxial strained (b) uxianal strained

Table 3 shows electrical characteristic of PMOS with embedded SiGe in the source/drain areas and SiGe layer deposited on bottom of strained silicon layer. From table 3 it shows that comparison on threshold voltage and drain current of conventional PMOS with two techniques strained such as uniaxial strained PMOS and biaxial strained PMOS were used to compare the electrical characteristic performance.

TABLE 3
ELECTRICAL CHARACTERISTIC WITH SILICON GERMANIUM

Electrical Characteristics	Conventional PMOS	Biaxial Strained PMOS	Uniaxial Strained PMOS
Vt (V)	-0.119	-0.135	-0.142
Id(mA)	-0.618	-0.739	-0.786

As seen from table 3, it can be seen the biaxial strained PMOS and uniaxial strained PMOS has lower threshold voltages. This is due to the narrowed band gap caused by the valance band shifting[8][9]. Thus the strained silicon PMOS can be switch on at lower value of gate voltage[8][9]. For uniaxial strained PMOS, it has lower threshold voltage than biaxial strained which is caused by the higher concentration of germanium content in uniaxial strained forming higher valence band voltage if compared to biaxial strained[8][9].

Figure 13 shows the comparison the drain current of conventional PMOS with biaxial strained and uniaxial strained.

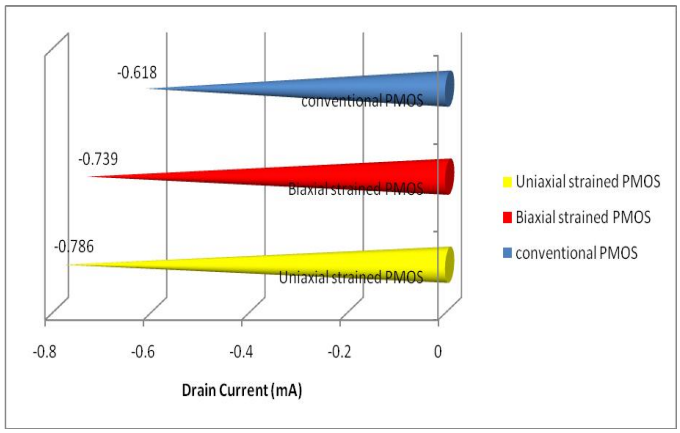

Fig. 13: Drain current comparison of conventional PMOS between biaxial strained and uniaxial strained.

From figure 13, the drain current for biaxial PMOS and uniaxial PMOS were improve. Biaxial strained PMOS improve 16.4% while uniaxial strained PMOS improve 21.4%. Thus, PMOS transistor shows the improvement when using silicon germanium. For strained technology, it can be concluded that an uniaxial strained and biaxial strained were the best strained for PMOS performance. An uniaxial strained PMOS having high compressive strain in the channel region than biaxial strained PMOS, thereby resulting in significant hole mobility improvement[10].

VI. CONCLUSION

Based on result, it can be concluded that strain technology is capable to improve the CMOS device performance. NMOS with Si_3N_4 capping layer tensile strain improve 46.9% drain current. However, variation of Si_3N_4 capping layer thickness does not shown any significant impact on electrical properties. This proved that Si_3N_4 film is the best strained technology on 90 nm for NMOS transistor.

PMOS transistor with embedded SiGe pocket in the source and drain areas improve 21.4% drain current while PMOS transistor with SiGe layer on bottom of strained silicon improve 16.4% drain current. An uniaxial strained and biaxial strained were the best strained for PMOS transistor performance but an uniaxial strained PMOS having high compressive strain than biaxial PMOS. This proved that uniaxial strained PMOS is the best strained technology on 90 nm for PMOS because uniaxial strained silicon transistor have demonstrated dramatic strain-induced performance gains[10]. Uniaxial strain is more effective, less costly and easier to implement relative to biaxial strain[10]. Uniaxial strain has significantly more advantageous effect on the valance band structure relative to biaxial stress which will likely make it the dominant strained silicon technology[10].

Overall, strained technology were the best on 90 nm for CMOS device is combination of Si_3N_4 film tensile strain for NMOS and uniaxial compressive strain for PMOS. For future development, the strained silicon on 90 nm CMOS devices can combine with silicon on insulator (SOI). From this combination of two technologies, strained silicon on insulator (SSOI) will be offers more improvement on drive current, faster switching times, reduced power consumption and lower voltage operation.

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REFERENCES

[1] K. Rim, J. Chu, H. Chen, K. A. Jenkins, T. Kanarsky, K. Lee, A. Mocuta,H. Zhu, R. Roy, J. Newbury, J. Ott, K. Petrarca, P. Mooney, D. Lacey, S.Koester, K. Chan, D. Boyd, M. Ieong, and H.-S. Wong, "strained-Si for sub-100-nm MOSFETs," *VLSI Symp. Tech. Dig.*, pp. 98–99, 2002.

[2] S. Thompson, N. Anand, M. Armstrong, C. Auth, B. Arcot, M. Alavi, P. Bai, J. Bielefeld, R. Bigwood, J. Brandenburg, M. Buehler, S. Cea, V. Chikarmane, C. Choi, R. Frankovic, T. Ghani, G. Glass, W. Han, T. Hoffmann, M. Hussein, P. Jacob, A. Jain, C. Jan, S. Joshi, C. Kenyon, J. Klaus, S. Klopcic, J. Luce, Z. Ma, B. Mcintyre, K. Mistry, A. Murthy, P. Nguyen, H. Pearson, T. Sandford, R. Schweinfurth, R. Shaheed, S. Sivakumar, M. Taylor, B. Tufts, C. Wallace, P. Wang, C. Weber, and M. Bohr, "A 90-nm logic technology featuring 50-nm strained-silicon channel transistors, 7 layers of Cu interconnects, low k ILD, and 1 _m /SRAM cell," in *IEDM Tech. Dig.*, 2002, pp. 61–64.

[3] S. Ito, H. Namba, K. Yamaguchi, T. Hirata, K. Ando, S. Koyama, S. Kuroki, N. Ikezawa, T. Suzuki, T. Saitoch, and T. Horiuchi, "Mechanical stress effect of etch-stop nitride and its impact on deep submicron transistor design," in *IEDM Tech. Dig.*, 2000, pp. 247–250.

[4] K. Rim, J. L. Hoyt, and J. F. Gibbons, "Fabrication and Analysis of Deep Submicron Strained-Si NMOSFET's," *IEEE Transactions on Electron Devices*, vol. 47, no. 7, pp. 1406–1415, 2000.

[5] S. Takagi *et al*., "Channel Structure Design, Fabrication and Carrier Transport Properties of Strained-Si/SiGe-On-Insulator (Strained-SOI) MOSFETs," in *IEDM Technical Digest*, Washington, DC, USA, pp. 57–60, December 2003.

[6] A.Shimizu, K.Hachimine, N.Ohki, M.Koguchi Y.Nonaka, H.Sato and F.Ootsuka, Local Mechanical-Stress Contro (LMC): A New Technique for CMOS Performance Enhancement, 2001

[7] K. Goto, S. Satoh, H. Ohta, S. Fukuta, T. Yamamoto, T. Mori, Y. Tagawa, T. Sakuma, T. Saiki, Y. Shimamune, A. Katakami, A. Hatada, H. Morioka, Y. Hayami, Shagaki, K. Kawamura and K. Hashimoto, Technology Booster using strain- Enhancing Laminated SiN (SELS) for 65 nm Node HP MPUs,2004

[8] Courtesy Jan Rabaey, "Mobility Enhancement The Next Vector to Extend Moore's Law," in IEEE Circuit & Devices Magazine, September/October 2005

[9] S.E. Thompson, M. Armstrong, C. Auth, M. Alavi, M. Buehler, R. Chau, S. Cea, T. Ghani, G. Glass, T. Hoffman, C.H jan, C. Kenyon, J. Klaus, K. Kuhn, Z. Ma, B. Mcintyre, K. Mistry, A. Murthy, B. Obradovic, Ramune Nagisetty, P. Nguyen, S. Sivakumar, R. Shadeed, L. Shifren, B. tufts, S. Tyagi, M.Bohr and Y.E. mansy, " A 90-nm Tecnology Featuring Strained-Silicon," Journal of IEEE Transaction on Electron devices, Volume 51, No.11, Retrieved August 23, 2009.

[10] T. Ghani, M.Armstrong, C. Auth, M. Giles, K. Mistry, A. Murthy, S. Thompson and M. Bohr, "Uniaxial Strained Silicon CMOS Devices for High Performance Logic Nanotechnology," in Portland Technology Development TCAD, Intel Corporation Hillsboro,OR.