Analysis and Optimization of 3 to 5 GHz CMOS Low Noise Amplifier for Ultra-Wideband (UWB) Systems

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***Abstract* – This paper presented analysis for a single stage Ultra-wideband CMOS Low Noise Amplifier interfacing interstage matching inductor cascade inductive source degeneration. Cadence design tool is used to optimize the simulation performance base on transistor size and inductor. The LNA is implemented using Siltera 0.18µm CMOS technology for a 3 to 5 GHz ultra-wideband system. By carefully optimization, size of transistor CMOS and an interstage inductor can increase the overall broadband gain while maintaining a low level of noise figure of an amplifier. The optimization of the LNA UWB has stability factor's more than 1, power gain +11.27dB and noise figure of 2.15 dB at frequency 4.5GHz.**

Keywords - Noise Figure (NF), Stability Factor (K), S-parameter, Gain

I. INTRODUCTION

Recently, the interest in ultra-wideband (UWB) system for high speed and high data-rate wireless communications has encouraged intensive research in both academic and industrial field. The allocated frequency band of the UWB system is 3.1 – 10.6 GHz: (low-frequency band 3.1-5 GHz, high-frequency band: 6-10.6GHz). Two major solutions, MB-OFDM based on frequency hopping and DS-UWB are proposed to transmit the data rate up to 480Mbps by using only the low frequency band. This frequency band (3168 MHz to 4752 MHz) is decided as the mandatory mode (Mode 1) for the development of the first-generation UWB system [1].

CMOS technology is satisfactory choice for the implementation of the low band UWB system when considering the time to market, hardware cost, and the degree of difficulty. Among that have been reported CMOS–based wideband amplifiers tend to be dominated by a few type of topologies such the distributed amplifier, resistive shunt-feedback amplifiers and multi stage cascade amplifier and also LC matching and filtering amplifier. The distributed amplifier [2], [3] provide wide bandwidth characteristic but it consume large dc due to the distribution of multiple amplifying stages, which makes them unsuitable for low-power application.

The resistive shunt-feedback-based amplifiers [4], [5] provide good wide band matching and flat gain, but tend to suffer from poor noise figure (NF) and large power dissipation. For the resistive shunt feedback amplifier, input resistance is determined by the feedback resistance divided by the loop-gain of the feedback amplifier. Therefore, the feedback resistor tends to be a few hundred ohms in order to match the low signal source resistance of typically 50 ohms, leading to significant NF degradation. In the meantime, even with a moderate amount of voltage gain, the amplifier requires a large amount of current; it is due to strong dependence for voltage gain on the transconductance of the amplifier transistor.

In a difference topologies such as LC matching and filtering amplifier that report in [6] and [7]. The band pass filter-based topology incorporates the input impedance of the cascade amplifier as part of the filter, and shows good performance while dissipating small amount of dc power. However, the adoption of the LC filter at the input mandates a number of reactive elements, which could lead to a larger chip area and NF degradation in the case of on-chip implementation, or the additional external components.

In this paper is the analysis and optimization of a modified single-stage cascade inductive LNA for UWB receiver using 0.18um standard RF CMOS process as shown in figure 1a is propose.

II. CIRCUIT ANALYSIS

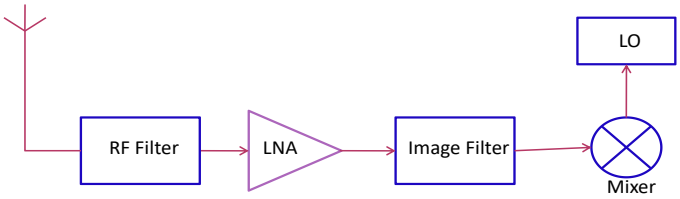

Diagram 1: Structure of LNA in front end

In this work that relies on the use of interstage inductor in order to achieve optimum noise figure and gain while maintaining a wideband bandwidth. The model LNA interstage is simulated and optimize by using Cadence design

tool. The model single stage cascade with interstage matching inductor LNA is shown in figure 1a. The modified cascade topology can be viewed as two stage amplifier configuration consisting of a common source (CS) stage, and inductor and a common gate (CG) stage as shown in Figure 1b.

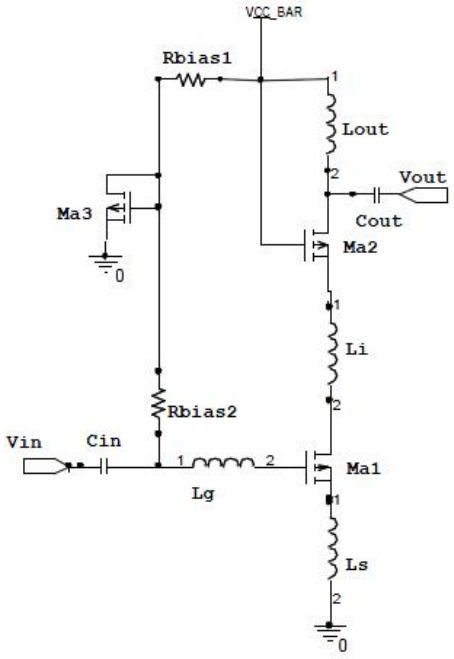

Figure 1a: Schematic of the model single-stage UWB LNA

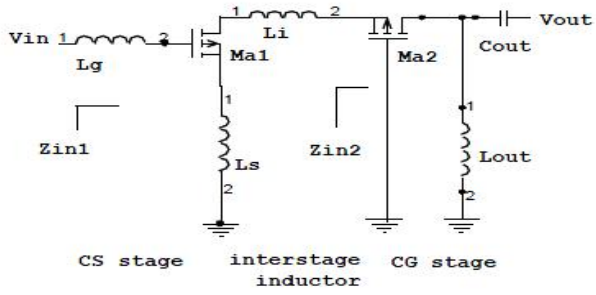

Figure 1b: The cascade topology of the UWB LNA

The CS stage is calculate to produce optimum gain at 3 GHz using inductive degeneration and the CG stage design with interstage matching inductor to produce optimum noise figure at 5GHz. In the CS stage, Zin is given by:

$$Zin = s.Lg + \frac{1}{s.Cgs} + s.Ls\left(\frac{gm}{s.Cgs} + 1\right), sub\ s = jw \text{ --- (1)}$$

$$Ra = gm\frac{Ls}{Cgs} \text{ --- (2)}$$

Where inductor Ls and Lg are the source degeneration inductor and the gate input inductor. And gm and Cgs are the transconductance and the gate-source capacitance of Ma1. The real part of the circuit is (2).

It is important to match the desired impedance with the Rs that can be obtained by setting Ls accordingly. Rs are given normally 50Ω, so, the imaginary part of the input impedance can be compensated with an input matching inductance Lg. In the CS stage, the source degeneration inductor Ls is there for simultaneous noise and input matching where as Lg is needed for the impedance matching between the source resistance (Rs=50Ω) and the input transistor Ma1 [8].

The inductor Ls need to be in the selected value since it will improve the linearity and the stability but at the same time it will reduces the gain of the LNA [8]. L*s* is important in stability of the LNA (for Rollet's stability factor, K > 1). The values of R_{bias2} and L_g are optimized carefully because they affect the overall gain of the CS stage [1].

In the CG stage, an inductor L_{out} of approximately 4nH is suitable to be place. The size of Ma2 also used to provide high gain of the amplifier at high frequency. By the way, large transistor size also will increase the power consumption and also increase the size of chip.

In addition, the value of interstage inductor L*i*, use to optimize for optimum gain and noise figure. Large value of L*i* will produces a high gain and low noise figure performance, but with the large chip area [8].

Finally, function of a capacitor C_{out} to be placed at the output as a dc block. The biasing networks were form by two resistors R_{bias1} and R_{bias2} and a transistor Ma_3. The component used in the design in the figure 1a is in the Table 1.

Component	Value	Units
L_g	3.5	nH
L_s	0.5	nH
L_i	1.5	nH
L_{out}	4	nH
R_{bias}	2k	Ω
Ma1, Ma2, Ma3	2.5/0.18(W/L) as per finger	µm
Ma1	150 (total size)	µm
Ma2	150	µm
Ma3	100	µm

Table 1: Value of the component in the simulation

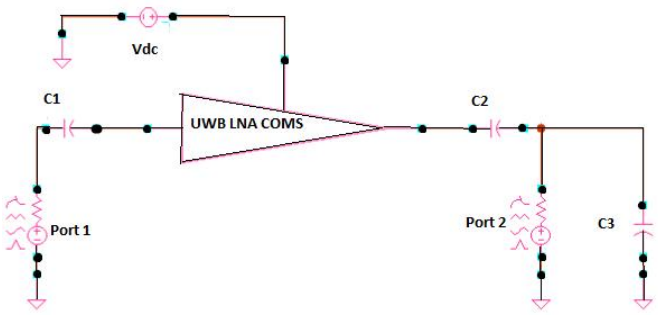

Figure 1c: Test bench of the LNA

III. Result and Discussion

All schematic are simulated according to the design. The design parameters are the length and the width of CMOS, value of inductor L*s* and L*i*, and the architecture of the low noise amplifier. These design parameters are very important to produce the expected result. All data of the simulation result are analyzed using Cadence tool. The standard specification of the ultra-wideband LNA are use to compare the result of the simulation as shown in table 2.

Parameter	Specification	Simulation	Units
Frequency	2.8-5	3-5	GHz
Noise Figure	4.5	2.13	dB
Gain	>10	12	dB
Stability Factor	>1	2.1	
Source/Load impedance	50	50	ohms
Voltage Supply	1.8	1.8	V

Table 2: Specification and simulated of UWB LNA.

a. Stability Factor, Kf

From figure 2 simulation result, stability factor will increase with the significant value of L*s*. So, the 0.5nH are the good inductor Ls to be selected since it stability greater than 1. The inductor Ls also will affect the overall gain significantly with the increase of L*s*.

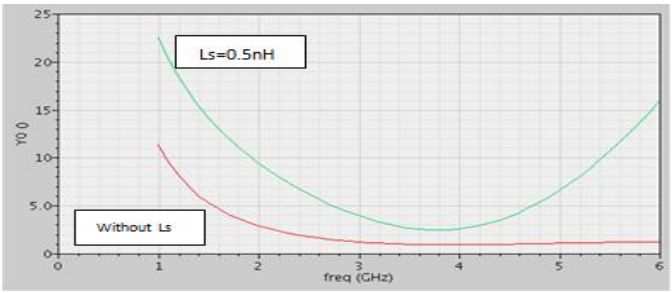

Figure 2: Stability of LNA represented by K greater than 1 with Ls.

b. Noise figure, NF and gain, G_A with the size of transistor Ma2

In order to make design have the specification, the size of transistor, Ma2 and inductor, L*i* must select carefully. From figure 3a and 3b, the common gate (CG) stage of the LNA will have high gain and low noise significantly with the increase of the transistor size, Ma2. But if the size increases, it will increase the area of transistor as discuss in paper [1]. Therefore, the transistor size for Ma2 is maintained at 150 µm for its moderate chip area and power consumption.

Size of Ma2	Noise Figure, dB	Gain, dB
50µm	10.16	2.47
100µm	4.6	7.51
150µm	2.16	11.89
200µm	1.276	14.97

Table 3: Simulated of the size Ma2 affect the noise figure and gain of the LNA.

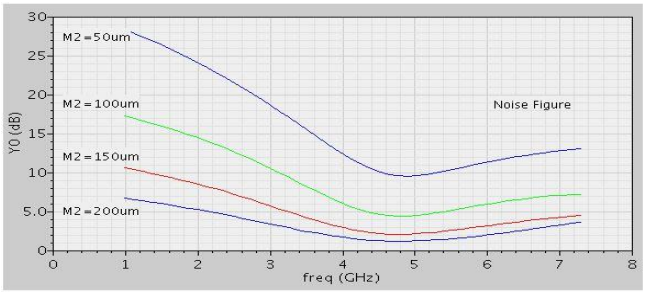

Figure 3a: Simulated frequency response over the noise figure, NF of the LNA with difference size of Ma2.

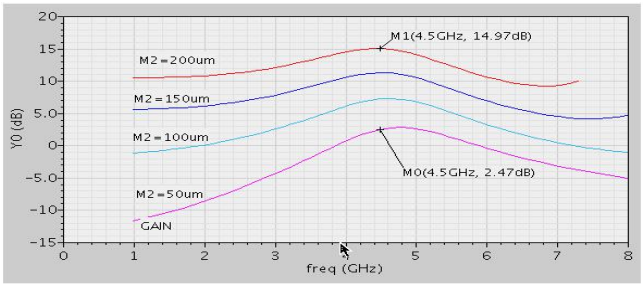

Figure 3b: Simulated frequency response over the gain, G_A of the LNA with difference size of Ma2

c. Noise figure, NF and gain, G_A, with the inductor Li

From the simulated as shown in figure 4, inductor L*i* also have to be choosing carefully, since the noise figure and gain is significant with the increase of the inductor, L*i*. With the larger inductor, the area of the chip also increases. Therefore, the inductor L*i* is 1.5nH to avoid increase area of the chip.

Li	Noise Figure (NF)	Gain (Ga)
1.0nH	4.52dB	6.6dB
1.5nH	4.201dB	7.0dB
2.0nH	3.887dB	7.4dB
3.0nH	3.274dB	7.9dB

Table 4: Simulated of the inductor, L*i* affect the noise figure and gain of the LNA.

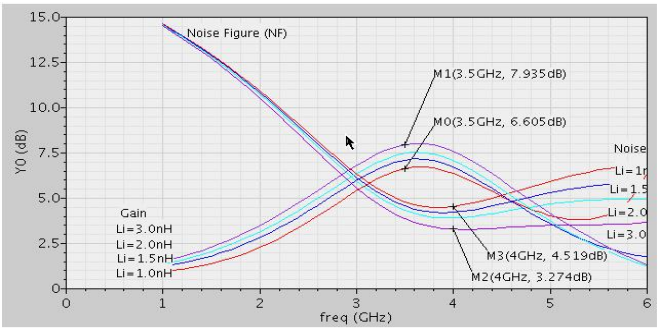

Figure 4: Simulated overall gain, G_A and noise figure with difference of the inductor L*i*.

d. Optimization simulation of the Ultra-wideband LNA

Finally, the analysis and optimization of the ultra-wideband LNA is to maximize the gain and low noise figure. The simulated in figure 3a and figure 3b have produce a good gain and noise figure with the size of transistor, Ma2 is 150µm. For the inductor L*i*, is 1.5nH have produce the high gain and lower noise with the small area of the chip as shown in figure 4. In figure 5, the simulation has been done after carefully selected total transistor size of Ma1 and Ma2, inductor L*s*, and inductor L*i* as in table 5.

Component	Value	Units
Lg	3.5	nH
Li	1.5	nH
Ls	0.5	nH
Ma1	150	µm
Ma2	150	µm

Table 5: Parameter of the components for the optimization Ultra-wideband LNA after the carefully selected.

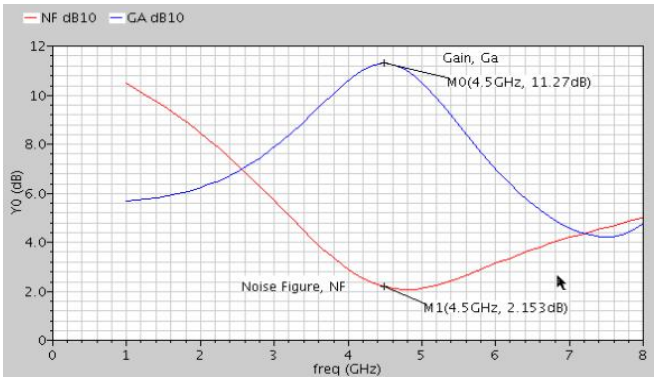

Figure 5: Simulated gain and noise figure of the LNA

IV. CONCLUSION

From the simulation, the design of the LNA was found to be able of generating fulfilling the gain and noise requirements of the ultra wideband (UWB) standard. The Ls need to be small for the LNA have the stability factor, K*f* that greater than 1, and good gain, G_A. The interstage inductor L*i* will affect the noise figure and gain, since when the inductor L*i* increase, gain increase and noise decrease, but at the same time, will generate large area of chip size. The size of the transistor Ma1 and Ma2 also have main important component to determine the noise figure and gain. Compared to other LNA techniques, the simulation ultra-wideband LNA has less design complexity with only four transistors in a single stage topology. For the future work, more study and understanding need to done to increase the gain and reduce the size and power consumption of the transistor.

V. ACKNOWLEDGMENT

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