Programmable Sample and Hold Circuit for Reconfigurable System

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***Abstract*—This project presents a sample and hold circuit design with four different frequency applications such as biomedical signal (16Hz-10MHz), radio frequency (<3kHz–300GHz), intermediate frequency (110kHz–1500MHz) and power (50Hz). The frequency applications will be the input to the sample and hold circuit of Silterra CMOS 0.13µm technology. The designed sample and hold circuit use 1.5V for the power supply and designed using Mentor Graphic tools. Total power dissipation for sample and hold circuit is 153.89µ Watts. The variety of frequency applications was used to obtain the different output signal for sample and hold circuit design before the signal is sent to the other system such as an analog digital converter (ADC).**

Keywords—Sample and Hold, Operational Amplifier, Mentor Graphic, Silterra CMOS 0.13µm Technology

I. INTRODUCTION

Reconfigurable system is a system that can be change or modified especially sub-system configurations. Reconfigurable devices, including field programmable gate arrays (FPGAs), contain an array of computational elements whose functionality is determined through multiple programmable configuration bits. These elements, sometimes known as logic blocks, are connected using a set of routing resources that are also programmable.

Programmable hardware is the core component in reconfigurable system, and it can be temporarily (partly) customized for a specific program or part of the program. Reconfigurability is divided by two categories, static and dynamic. Analog-to-digital converters (ADCs) are important building blocks in modern signal processing and communication systems. There are many types of ADC such as flash ADC, folding and interpolating ADC, pipeline ADC, delta-sigma ADC and integrating ADC [1]. The pipelined ADC is one of the types of ADC, which is having a lot of advantages. One of the benefits, it is being an alternative solution for wireless communication system. Pipelined ADC consists of several components, which are the coarse and fine ADCs, sample and hold circuit (S/H), digital-to-analog converter (DAC) and the interstate amplifier.

Other work on sample and hold circuit mostly applied fixed frequency in the input to the sample and hold circuit. In this paper [2], focused on 5 MHz sampling frequency with considering 1.2 V_{pp}. Other findings are using 125 MHz input sinusoidal signal with a 0.8 V_{pp} [3].

Sample-and-hold circuit is an important part in the pipeline ADC architecture and other data-converter systems. The conversion process of pipelined ADC begins with sample-and-hold circuit [2]. The sample and hold circuits can be substantially divided into two categories, closed-loop S/H and open-loop S/H. For applications requiring high accuracy, one can use the closed loop-architecture, with follower output and an integrator output. The feedback significantly improves the accuracy of the sample and hold, although the speed is somewhat less [4]. The operation of sample and hold circuit is divided into two phase which is the sampling phase and hold phase. In this paper, the main application of this sample and hold circuit is to get the variety of output with different frequency that enter the systems.

This paper is divided into seven main parts. In section 2, methodology of the project. Section 3 is the design architecture and procedure of sample and hold circuit. In section 4, simulation result and discussion. Section 5 is layout design and section 6 is about post layout simulation of sample and hold circuit and operational amplifier. Finally, section 7 concludes the work of sample and hold circuit design.

II. METHODOLOGY

A. Flow Chart

Figure 1 shows the flow chart of the design for operational amplifier using 0.13µm technology with Mentor Graphic tools. The op-amp is designed with the parameter or specification and then analyzed the waveform to get the phase margin and dc gain before proceed with the layout. The project was ending

with layout verification using design rule check (DRC), layout versus schematic check (LVS) and lastly for parasitic extraction (PEX).

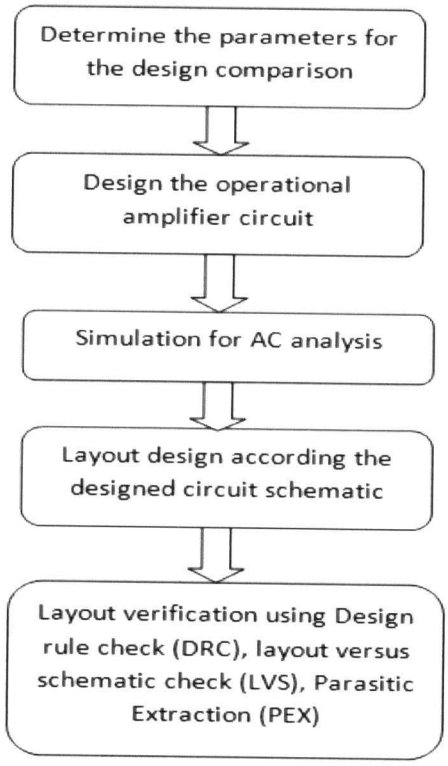

Figure 1. Flow Chart of the design of operational amplifier

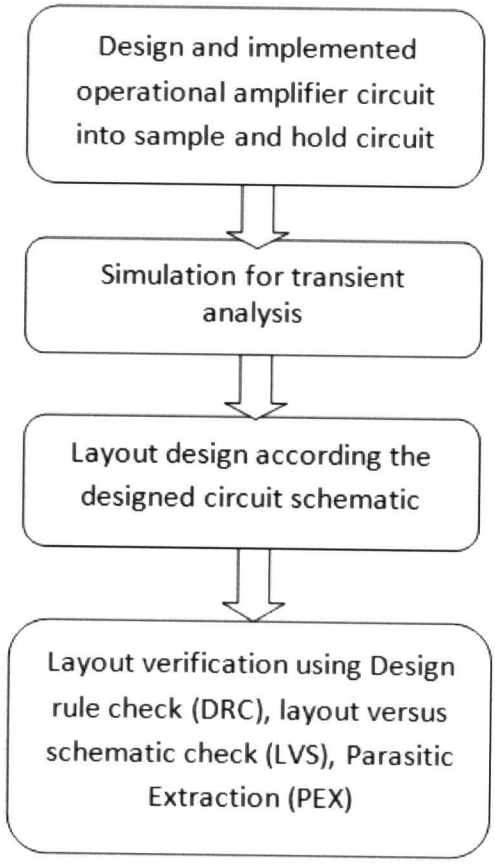

Figure 2. Flow chart of the sample and hold circuit design

The different frequency, such as biomedical signal, radio frequency, intermediate frequency and power enter the input of sample and hold circuit design, the process will be executed based on the Figure 2.

III. DESIGN ARCHITECTURE AND PROCEDURE

A simple sampling switch show in Figure 3 about a nMOS transistor and a holding capacitor. When switch is on, the CLK goes high followed with V_{in} and when switch is off, CLK goes low V_{out} is remains constant [5].

In this work the sample and hold circuit are using operational amplifier, switching nMOS (M2 and M3) and transmission gate (M1) as shown in Figure 4.

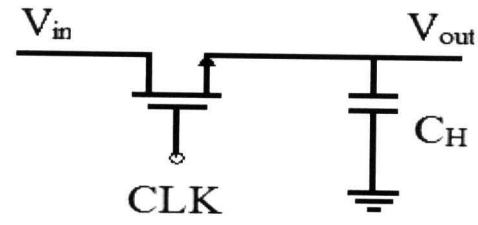

Figure 3. A simple sampling switch

The main part of designing sample and hold circuit are operational amplifier (op-amp). There are many types of fully differential op-amps such as telescopic, gain boosted, folded-cascode and multi-stage op amps [6].

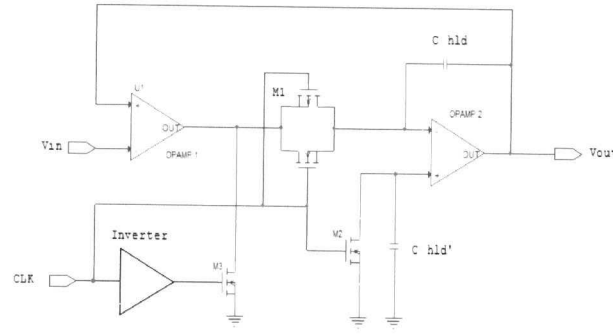

Figure 4. Schematic sample and hold circuit

Figure 4 depicts the proposed op-amp used in this work. In order to achieve high gain and design a low power consumption, multi-stage amplifier are recommended [2].

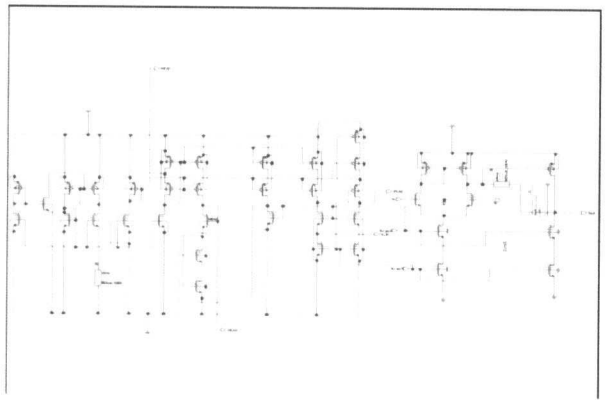

Figure 5. Multi-stage operational amplifier

The operational amplifier are designed in a low power consumption using 1.5 V power supply in Silterra CMOS 0.13µm technology. This is because if power dissipation is reduced the power will be able to provide more space for the signal and to keep the same signal-to-noise ratio [7].

Figure 6 shows the sample and hold circuit designed using Silterra CMOS 0.13µm technology with 1.5V power supply. The circuit consist of two op-amps : Op-amp 1 and op-amp 2. The op-amp 1 is used to amplified the frequency input used in this work to be sampled. The hold capacitor is placed in the feedback path of a second op-amp. So that, both side of transmission gate is almost signal independent if op-amp 2 has a large gain. The input differential voltage of sample and hold circuit can be described as [2]:

$$V_{in} = V_{in+} - V_{in-} \quad (1)$$

For the output differential voltage of sample and hold circuit can be defined by :

$$V_{out} = V_{out+} - V_{out-} \quad (2)$$

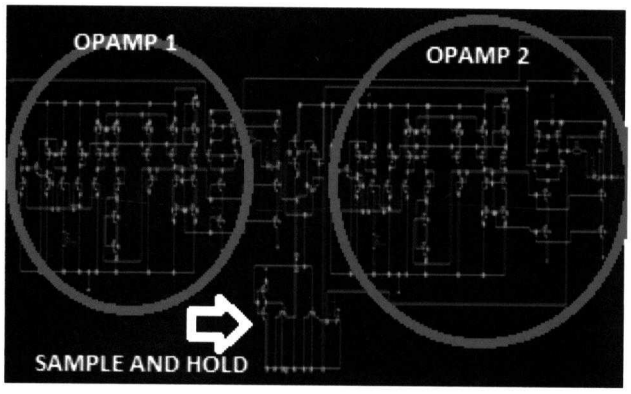

Figure 6. Schematic circuit of sample and hold

IV. RESULT AND DISCUSSION

In this section, there are two parts of schematic simulation results which are the simulation output of op-amp and sample and hold circuit.

A. Simulation of Operational Amplifier

The simulation result is analyzed using AC analysis is shown in Figure 7 using Mentor Graphic tools. The op-amp specifications are summarized in table 1 with supply voltage 1.5V. It is difficult to obtain a constant g_m and hence a constant gain-bandwidth product over the full input range [8].

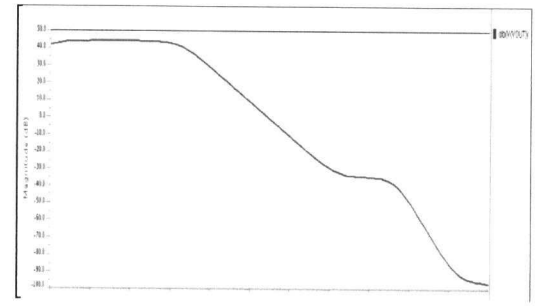

Figure 7. Simulation result of AC analysis of op-amp

TABLE 1. DESIGN SPECIFICATIONS OF OP-AMP

Design Specificatios	Pre-layout value	Post-layout value
CMOS Technology	0.13µm	0.13µm
Power Consumption	0.179mW	0.166mW
DC Gain	64.898 dB	66.565 dB
Phase Margin	91.373 °	91.252 °

From the result, it shows that the power consumption is reduced after doing parasitic extraction (PEX). It also increased the DC gain and phase margin is reduced. This is because the effect of parasitic in the design.

B. Simulation of sample and hold circuit

Figure 8 shows the output of the sample and hold circuit tested with 5 MHz sinusoidal input signal. The frequency is sampled at 50 MHz with 1.2 Vpp. The result revealed that it does not exactly match the input signal. It showed that the output is referred to voltage reference, V_{ref} is equal to 0.83 V. This findings has been similar to work done by [2]. This result is not exactly match with the other work or ideal simulation output because of the value chain in the op-amp has dropped in the second op-amp. This maybe affect at the biasing value in the op-amp itself. It's also affected by the parasitic capacitance after doing simulation.

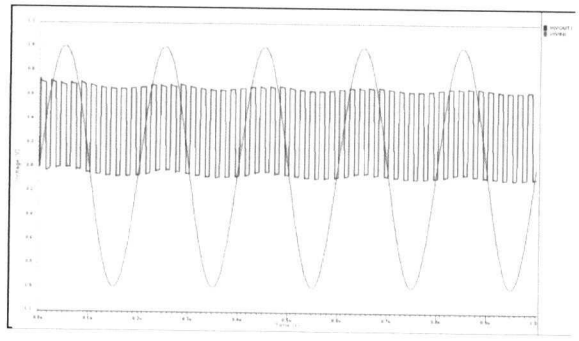

Figure 8. Simulation output from sample and hold circuit

The different frequencies was sampled on the sample and hold circuit from lower frequency (20 Hz) until high frequency (5 GHz) show in Figure 9. The different frequency applications based on biomedical signal (16 Hz-10 MHz) [9, 10], radio frequency (3 kHz–300 GHz) [9], intermediate frequency (110 kHz–1500 MHz) [11] and power (35.9 kHz-90.6 kHz) [12].

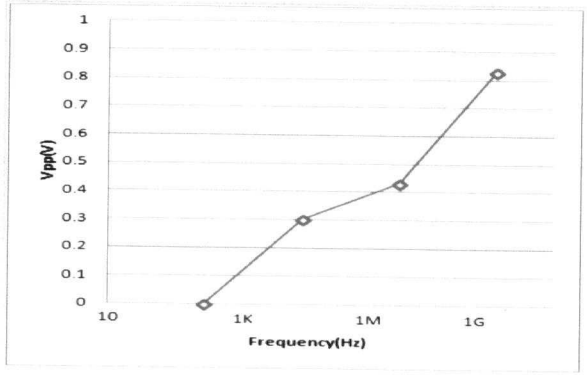

Figure 9. Simulation output of sample and hold circuit

The Figure 9 shows that the voltage peak-to-peak (Vpp) direct proportional with the frequency (Hz).

V. LAYOUT DESIGN

Figure 10 and 11 show the layout design of operational amplifier and sample and hold circuit using CMOS 0.13µm technology and designed using Mentor Graphic tools. Both layouts passed the design rule check (DRC), layout versus schematic (LVS) and parasitic (PEX).

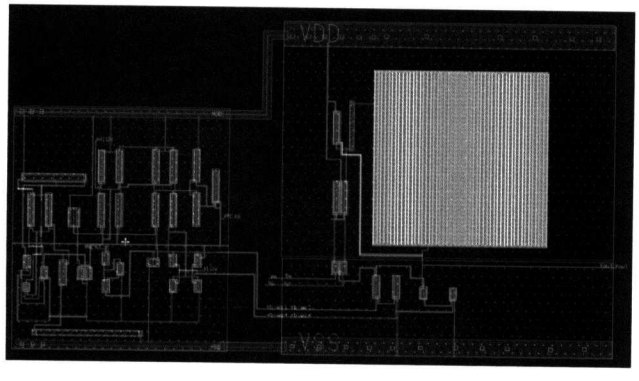

Figure 10. Layout design of operational amplifier

The performance for the whole process of operational amplifier is shown in Table 1. It shows that, the power reduced after parasitic extraction (PEX) this is because the effect of the parasitic on the design.

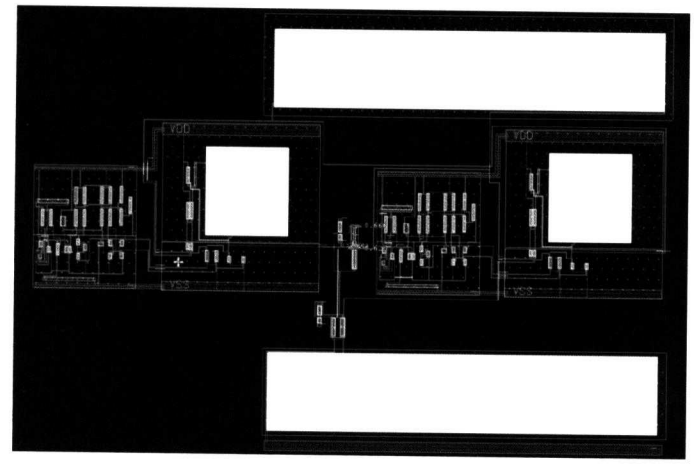

Figure 11. Layout design of sample and hold circuit

Figure 11 shows the layout design for sample and hold circuit. The total power dissipation for this circuit is 153.89µ Watts.

VI. CONCLUSION

In this paper, the frequency is varied from lower to higher frequency that enter the sample and hold design architecture can produce varies voltage peak-to-peak. The design is simulated using Silterra 0.13µm CMOS technology and operated with 1.5V of power supply. The simulation results of the sample and hold circuit indicates voltage peak-to-peak is directly proportional with frequency. For high frequency, the output waveform becomes large and this phenomenon can affect the value parasitic [13]. Finally, the sample and hold circuit can be used to implement with other circuit before entering the analog to digital circuit. Total power dissipation for sample and hold circuit is 153.89µ Watts.

ACKNOWLEDGEMENT

I would like to acknowledge En Abdul Hadi bin Abdul Razak and also Dr Suhana Sulaiman as supervisor for their time and idea in order to complete this project.

REFERENCES

[1] J. Li, "Accuracy enhancement techniques in low-voltage high-speed pipelined ADC design," 2003.

[2] S. L. M. Hassan, I. S. A. Halim, N. B. A. Aziz, and T. N. T. Yaakub, "Comparative study on multistage amplifier and folded cascode amplifier design in sample and hold circuit using 0.18µm CMOS technology," in *Computer Applications and Industrial Electronics (ISCAIE), 2012 IEEE Symposium on*, 2012, pp. 29-34.

[3] M. Hasan-Sagha and M. Jalali, "Very high speed and low voltage open-loop dual edge triggered sample and hold circuit in 0.18µm CMOS technology," in *Semiconductor Electronics (ICSE), 2012 10th IEEE International Conference on*, 2012, pp. 645-648.

[4] T. INSTRUMENTS, "Application Note 775 Specifications and Architectures of Sample-and-Hold Amplifiers," JULY 1992.

[5] M. Hasan-Sagha and M. Jalali, "Electr. & Comput. Eng. Dept., Shahed Univ., Tehran, Iran," in *Semiconductor Electronics (ICSE), 2012 10th IEEE International Conference on*, 2012, pp. 645-648.

[6] Z. Liu, C. Bian, Z. Wang, and C. Zhang, "Full custom design of a two-stage fully differential CMOS amplifier with high unity-gain bandwidth and large dynamic range at output," in *Circuits and Systems, 2005. 48th Midwest Symposium on*, 2005, pp. 984-987.

[7] R. Lotfi, M. Taherzadeh-Sani, M. Y. Azizi, and O. Shoaei, "Low-power design techniques for low-voltage fast-settling operational amplifiers in switched-capacitor applications," *Integration, the VLSI journal,* vol. 36, pp. 175-189, 2003.

[8] W. Sansen, "Analog circuit design in scaled CMOS technology," in *VLSI Circuits, 1996. Digest of Technical Papers., 1996 Symposium on*, 1996, pp. 8-11.

[9] R. Van Der Togt, E. J. van Lieshout, R. Hensbroek, E. Beinat, J. Binnekade, and P. Bakker, "Electromagnetic interference from radio frequency identification inducing potentially hazardous incidents in critical care medical equipment," *Jama,* vol. 299, pp. 2884-2890, 2008.

[10] X. Zou, X. Xu, L. Yao, and Y. Lian, "A 1-V 450-nW fully integrated programmable biomedical sensor interface chip," *Solid-State Circuits, IEEE Journal of,* vol. 44, pp. 1067-1077, 2009.

[11] S. Nakasono, M. Ikehata, M. Dateki, S. Yoshie, T. Shigemitsu, and T. Negishi, "Intermediate frequency magnetic fields do not have mutagenic, co-mutagenic or gene conversion potentials in microbial genotoxicity tests," *Mutation Research/Genetic Toxicology and Environmental Mutagenesis,* vol. 649, pp. 187-200, 2008.

[12] K. Razazian, M. Umari, A. Kamalizad, V. Loginov, and M. Navid, "G3-PLC specification for powerline communication: Overview, system simulation and field trial results," in *Power Line Communications and Its Applications (ISPLC), 2010 IEEE International Symposium on*, 2010, pp. 313-318.

[13] Z. Lin and Q.-X. Chu, "A novel approach to the design of dual-band power divider with variable power dividing ratio based on coupled-lines," *Progress In Electromagnetics Research,* vol. 103, pp. 271-284, 2010.