DESIGN A COMPARATOR OF 8-BIT ANALOGUE-TO-DIGITAL CONVERTER (ADC) IN A 0.35µm CMOS TECHNOLOGY BY USING MENTOR GRAPHICS

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ABSTRACT

A high performance on-chip comparator of 8-bit Analogue-To-Digital Converter (ADC) has been designed in a 0.35µm Complementary Metal Oxide Semiconductor (CMOS) Technology process. Full custom design flow is implemented in which the design starts with schematic entry followed by simulation for characterization purpose and validation. The IC layout of the comparator is achieved along with the post layout simulation and layout verification. The designed comparator is tested in an 8-bit ADC by simulation to determine the functionality and performance.

The comparator can handle positive and negative input signals. A polarity signal changes the polarity of the threshold level and makes the output signal always active high. The design is based on basic comparator architecture which consists of three stage; pre-amp, decision circuit and output buffer.

The results that were obtained through these simulations showed that comparator design achieved power consumption of 958.69µW, with supply voltage of 5V. Further research on the MOSFETs W/L factor has successfully improved the characteristics of the comparator to perform for the offset of 620µV. The uses of a latch as the positive feedback decision circuit and the improvement in offset have contributed to the speed performance of the comparator to achieve propagation delay of 3.52ns.

1.0. INTRODUCTION

A good ADC requires a high-performance comparator since the comparator will determine the accuracy of the ADC conversion. There are many circuit configurations of comparators for different applications with different characteristics. Although the basic op-amp configuration can be used as a voltage comparator, in some less demanding low-frequency or speed applications, op-amp will not be considered as a comparator.

In ADC, the gain and offset of a comparator will also contribute to the comparator speed improvement [1]. Hence, it is important to have a comparator with very good characteristics without consuming large amounts of power. The best approach to achieve such requirements is to employ an architecture which contains a preamplifier stage, positive feedback stage and output buffer stage. By implementing this architecture, the comparator can be easily characterized to satisfy the ADC requirements.

2.0. COMPARATOR DESIGN

2.1. Basic comparator

A comparator is a differential amplifier that compares the analog signals present at its input and produce logic output as the result of the comparison. Hence, it is also called decision-making circuit. The circuit symbol and ideal transfer function of a non-inverting comparator is shown in Figure 2.0 It can be seen that if the voltage difference $V_{IN+} - V_{IN-}$ is positive the comparator's output will go high, otherwise its output will go low.

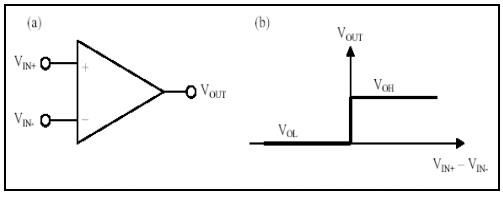

Figure 2.0: Comparator (a) circuit symbol (b) ideal transfer function

2.2. Performance Metrics

Resolution is the minimum input difference that can be resolved by the comparator in order to switch between its binary states. It is usually limited by the input-referred offset and noise generated by the internal components of the comparator.

The gain, Av, is one of the key limiting factors in achieving the desired resolution for the comparator. To obtain the ideal response shown in Figure 2.0, a transition between output logic levels occurs for a zero-input difference. This leads to a gain that approaches infinity, as given by the following equation,

$$A_V = \lim_{\Delta V \to 0} \frac{V_{OH} - V_{OL}}{\Delta V} \quad (1)$$

A real comparator has a finite gain as shown in figure 2.1, given by

$$A_V = \frac{V_{OH} - V_{OL}}{V_{IN+} - V_{IN-}} \quad (2)$$

The offset is a non-ideal effect that limits the resolution of the comparator. Assuming an ideal comparator with zero differential input voltage required to produce an output transition, the offset is defined as the minimum amount of input voltage required for the binary-state transition to take place. In a real comparator the offset adds to the minimum voltage for which the resolution was designed reducing the resolution of the circuit [2]. An illustration of how it affects the response of the circuit is given in Figure 2.1.

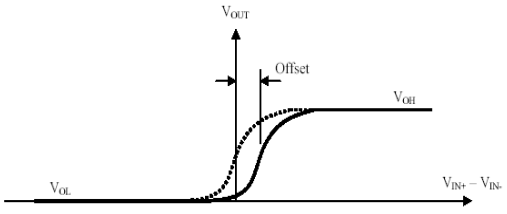

Figure 2.1: Non-ideal transfer function of comparator

The speed of a comparator is determined by the propagation delay and the settling time. The propagation delay is the time that elapses between an input transition and the corresponding output change. As shown in Figure 2.2, it is usually measured at the midpoints between the input and output signals.

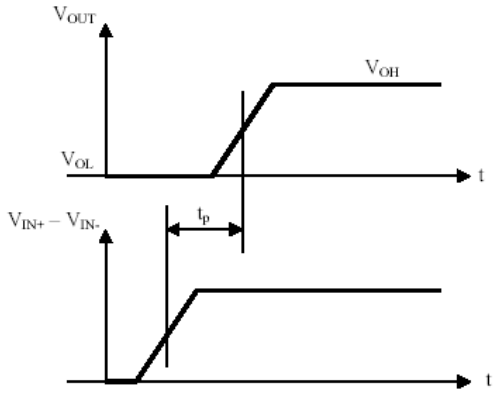

Figure 2.2: Propagation delay in a comparator

2.3. MOS Equation

Gate capacitance,

$$C_G = \frac{\varepsilon_{ox} A}{\tau_{ox}} \quad (3)$$

Oxide capacitance per unit area,

$$C_{ox} = \frac{\varepsilon_{ox}}{\tau_{ox}} \quad (4)$$

Channel length and channel width,

$$\frac{\beta_n}{\beta_p} = r \frac{\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_p} \quad (5)$$

$$\left(\frac{W}{L}\right)_{n,p} = \frac{2I_D}{\mu C_{ox} V_{o,sat}^2} \quad (6)$$

Parasitic resistance,

$$R_n \propto \frac{1}{\beta_n} \quad (7)$$

$$R_n = \frac{2}{\beta_n (V_{DD} - V_{Tn})} \quad (8)$$

2.4. Proposed Circuit

The comparator design is based on the basic comparator architecture which consists of three stage; pre-amplifier, decision circuit and output buffer. This architecture provides both good gain and offset characteristics by combining the pre-amp stage and the positive feedback decision circuit.

2.4.1. Pre-amplifier

The pre-amplifier stage amplifies the input signal that improves the comparator sensitivity and it also increase the minimum input signal which the comparator can make decision. Figure 2.3 shows the pre-amplifier schematic diagram

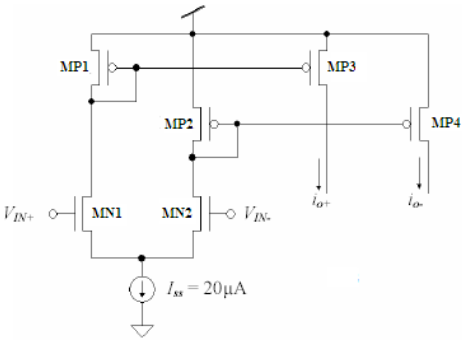

Figure 2.3: Pre-amplifier

2.4.2. Positive feedback decision circuit

The positive feedback is used to determine which of the input signals is larger and to decide which one the mV level signals. The positive feedback decision circuit is shown in Figure 2.4

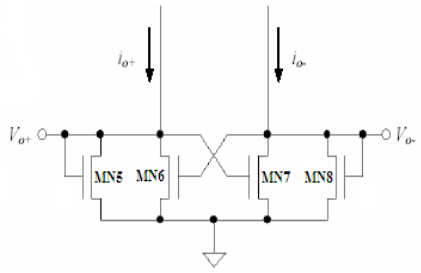

Figure 2.4: The output of positive feedback decision circuit

2.4.3. Current source

The differential amplifier needs a current source to provide constant current I_{ss} = 20µA. Current mirror circuit configuration as shown in Figure 4.3 is used. The width selection of MN3 and MN4 will not affect the comparator performance and hence, they are set to 5λ.

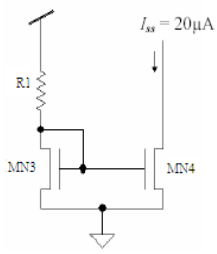

Figure 2.5: Current source for the different amplifier

By assuming V_{GS} = 0.9V, the resistor *R1* value is calculated to have the desired current I_{ss};

$$R_1 = \frac{V_{DD} - V_{GS}}{I_{SS}} \quad (10)$$

$$R_1 = \frac{5V - 0.9V}{20\mu A} = 205k\Omega$$

2.4.4. Output Buffer

Output buffer is needed at the final stage of the comparator to convert the output of the decision circuit which is varied 0.7935mV for "LOW" and 1.86145V for "HIGH" level into a logic signal that is 0 and 5V. An inverter was added on the output as shown in the Figure 2.6 as an additional gain stage and to isolate any load capacitance from the self-biasing differential amplifier.

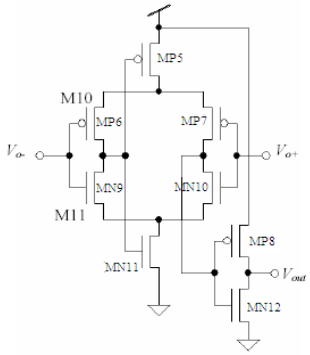

Figure 2.6: A comparator output buffer added an inverter

2.4.5. Complete circuit of a comparator

The design is based on basic architecture consists of pre-amp, decision circuit and output buffer. The combination of these three stages has brought the gain and offset improvement of the comparator. Another important factor that contributes to the performance of the comparator is the MOSFETs sizing or W/L.

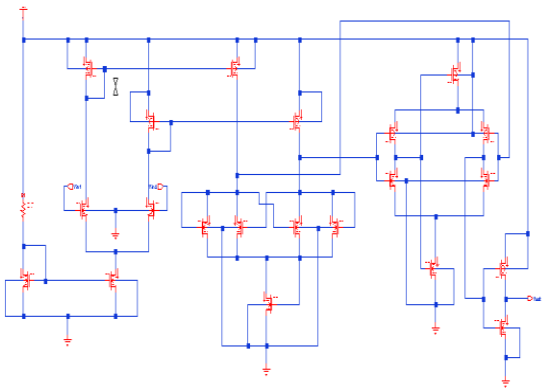

Figure 2.9: Complete schematic of the comparator

Circuit Blocks	Transistor device	W (λ)	L (λ)
Pre-amp	MP1,MP2,MP3,MP4	5	2
	MN1,MN2	10	2
Decision circuit	MN5,MN6,MN7,MN8	5	2
	MN13	8	2
Output buffer	MP5,MP6,MP7,MP8	5	2
	MN9,MN10,MN11, MN12	5	2
Current source	MN3,MN4	5	2

Table 2.0: Design parameter for the comparator

3.0. METHODOLOGY

The CMOS circuit design process consists of defining circuit inputs and outputs, hand calculations, circuit simulations, layout of the circuit, simulations including parasitic resistances, reevaluation of the circuit inputs and outputs and testing.

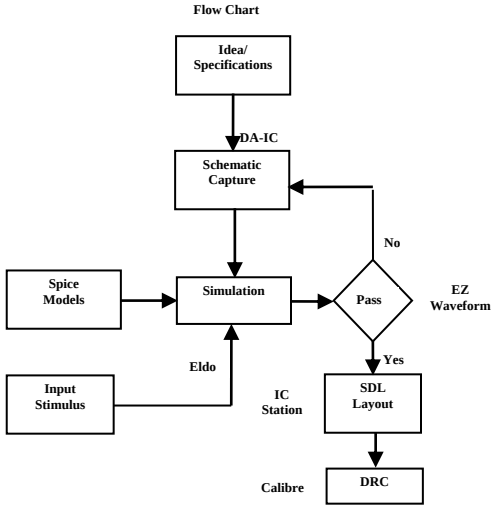

Figure 3.0: Flow chart of process designing the comparator.

The design is worked with full-custom design approach, the methodology that commonly been used by most analog IC designers. The design flow as shown in Figure 3.0 is started with schematic entry in which the schematic is designed and drawn in Design Architect-IC (DA-IC) which contains a function of a schematic capture, netlisting, and simulation setup/results viewing. It only can operate on Linux OS with full UNIX data compatibility and it can quickly output designs in SPICE, HSPICE, or verilog netlist formats. The designed schematic is then simulated and during this step, the comparator is characterized.

Eldo is an advanced analysis options such as transient noise, pole-zero, enhanced Monte-Carlo analysis, optimization, sensitivity, DC mismatch, loop stability analysis. It uses to integrate into Mentor Graphics' IC Flow.

After the schematic is simulated and the appropriate specification is achieved, the layout is constructed by using IC Station SDL which is a polygon editing functionality of ICgraph Basic, plus hierarchical, schematic-driven layout environment that allows designers to create IC layouts based on information from a logic source and makes navigation between the layout and schematic fast and easy based on the lambda design rule. Design Rule Check (DRC) is carried out to check whether the layout satisfies the specified design rule.

For the DRC, the layout is then extracted for post layout simulation purpose and this step will produce the layout netlist. IC Station SDL is used for all simulations involved through the design process.

4.0 RESULT AND DISCUSSION

4.1. Comparator characteristic

The characteristics of the comparator are investigated and improved through simulation. According to the 0.35µm SCN3M SCMOS design rule, the minimum width of the MOSFETs in analog application is 5λ to have optimum performance [6]. Test the performance of the comparator, DC analysis and transient analysis are carried out.

4.2. Comparator analysis

4.2.1. Comparator Gain and Offset

DC analysis is carried out to investigate the offset of the comparator. The input voltage V_{in+} is swept from 2.49 to 2.51V with V_{in-} is held at 2.5V, and V_{out} is plotted. The testbench or simulation profile for the analysis is as follow:

V2 VIN1 GND DC 2.5V
V3 VIN2 GND DC 2.5V
V1 VDD GND DC 5V
X COMPARATOR2 VIN1 VIN2 VOUT COMPARATOR2

The transfer curve of DC analysis result is shown in Figure 4.1. From the transfer curve, it is found that the systematic offset voltage of the comparator is approximately 620µV. This near-zero offset is the most important characteristic of the designed comparator since it can provide better quantization error of the ADC.

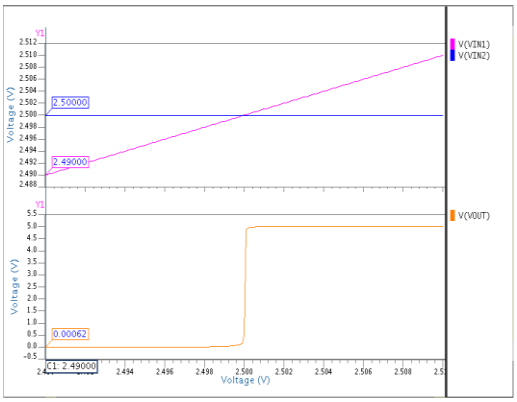

Figure 4.1: The transfer curve of the designed comparator

4.2.2. Transient Analysis

Transient response of a comparator can be significantly more difficult to characterize than the DC characteristics. For this test, V_{in-} is held at 2.5V while a 20ns wide pulse with amplitude 2.5V is inputted to the V_{in+}. The testbench or simulation profile for this transient analysis is as follow:

V2 VIN1 GND PULSE (0V 2.5V 1nS 1nS 1nS 20nS 50nS)
V3 VIN2 GND DC 2.5V
V1 VDD GND DC 5V
X_COMPARATOR21 VIN1 VIN2 VOUT COMPARATOR2

The simulation results shown that the comparator can successfully resolve differences of 10mV at 100MHz. If the pulse amplitude or width is reduced much beyond this, the comparator does not make full transition. Figure 4.2 and 4.3 shows the transient analysis results of the comparator. From the transient waveform, the V_{OL} and V_{OH} are obtained at 55.67mV and 4.73V respectively. While the propagation delay is calculated by

$$T_P = \frac{T_{pLH} + T_{pHL}}{2} \quad (11)$$

Propagation delay is refers to the delay time from input to output. From the transient waveform, T_{pLH} = 3.93ns and T_{pHL} = 3.11ns, and hence, the propagation delay, T_P of the comparator is 3.52ns.

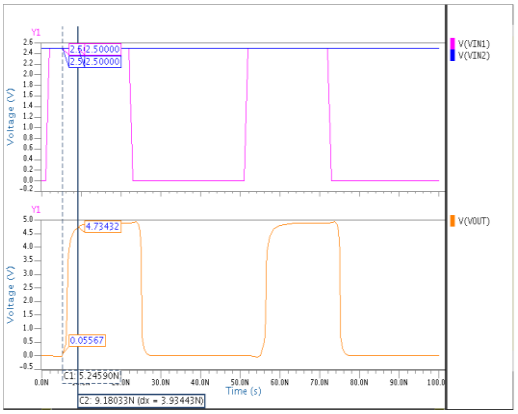

Figure 4.2: Transient response of the comparator for the T_{pLH}

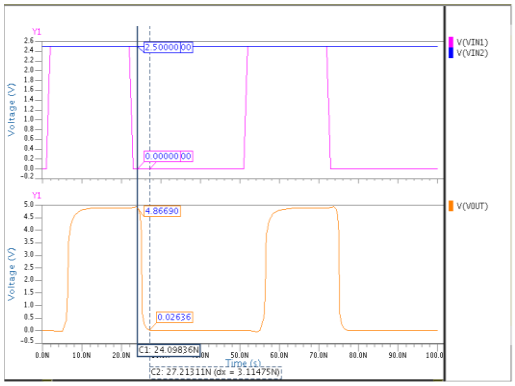

Figure 4.3: Transient response of the comparator for the T_{pHL}

4.2.3. Time Fall and Time Rise Analysis

From the comparator that have been designed, time fall and time rise are investigate by transient analysis that produce output waveform of the comparator.

Figure 4.4 and 4.5 show the output waveform of the comparator that satisfies the truth table of the comparator and shows before and after change the width of the transistors that the time fall and time rise are different. After change the width of the transistor, the time fall and time rise have been improve.

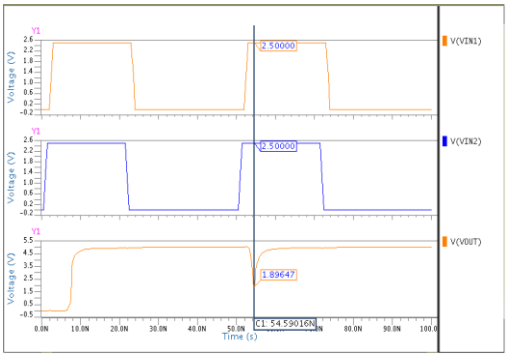

Figure 4.4: Output waveform of the comparator before change the width of the trans

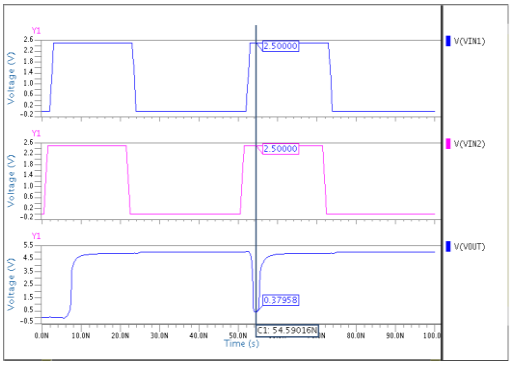

Figure 4.5: Output waveform of the comparator after change the width of the transistor

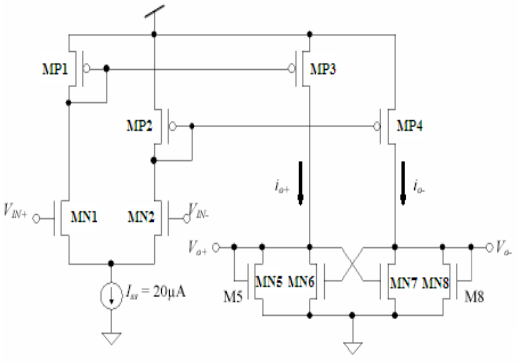

Figure 4.6: Schematic diagram of pre-amplifier and decision circuit

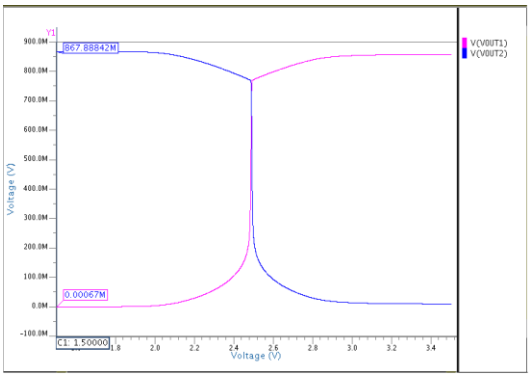

Figure 4.7: Transition circuit of pre-amplifier and decision circuit

4.2.4. Interfacing Pre-amplifier with Decision Circuit

At this point, the pre-amplifier and the decision circuit as shown in Figure 5.8 basically can operate as a comparator since it is able to discriminate the difference between the inverting and non inverting input (*Vin+* and *Vin-*) of the preamp and output voltage of decision circuit (*Vo+* and *Vo-*) determine the decision of which input voltage is larger. *Vo+* will raised to "HIGH" level when *Vin+* is larger than *Vin-* and drop to "LOW" level when *Vin+* is smaller than *Vin-*. *Vo-* is the complement to *Vin+*.

By simulation, the output transition characteristic of the circuit in Figure 4.6 is investigated. *Vin+* is swept from 1.5V to 3.5V while *Vin-* is held at 2.5V. The waveform of the simulation result is shown in Figure 4.7.

From simulation waveform result as shown in Figure 4.7, it is found that the output voltage levels from the positive feedback decision circuit stage are 0.00067mV for "LOW" level and 867.8824mV for "HIGH" level. The switching point is exactly happens when both input voltages are equal to 2.5V and it is important to have a good offset characteristic for a comparator. The width of MN5, MN6, MN7 and MN8 must be the same. If the width of MN5 and MN6 are different than the MN7 and MN8, it will be much affected to the switching point since the β is depend on the width of the MOSFETs and β parameter determines the conductivity of the MOSFETs during the triode operation.

To shift the output of the decision circuit up approximately 1V, the MOSFETs MN13 is added in series with the decision circuit as shown in Figure 4.8 where the MOSFETs will provide increment of the average voltage out of the decision circuit by approximately V_{THN}

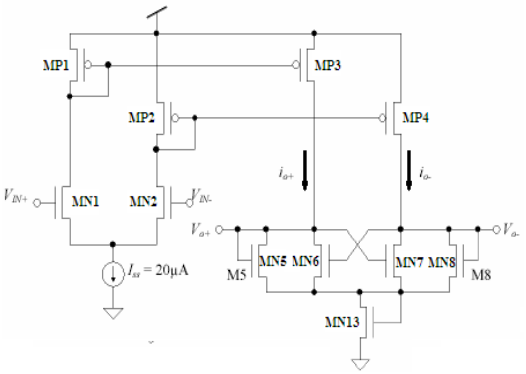

Figure 4.8: Schematic diagram of pre-amplifier and decision circuit by adding MN13 transistor

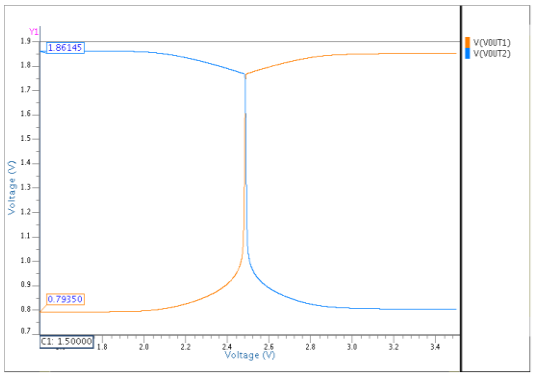

Figure 4.9: Transition circuit of pre-amplifier and decision circuit after adding MN13 transistor

The transition of the decision circuit output after adding MN13 is shown in Figure 4.9. The output voltage levels from the decision circuit stage are improved so that they lie between 0.79350mV for "LOW" level and 1.86145V for "HIGH" level.

Instead of providing output level shifting, it is found that the width of MN13 transistor will contribute to the offset characterization of the comparator, and hence it is set to 8λ to provide near-zero offset.

4.2.5. Comparator IC Layout Design

The design is based on 0.35µm CMOS Technology. Lambda design rule is used, in which the lambda, λ is set to 0.35µm. λ represents half the minimum drawn channel length allowed in the design rule. A set of lambda rules can be applied to different processes. For a particular process, the value for lambda is defined. According to the SCN3M SCMOS design rule, the minimum width of the MOSFETs in analog application is 5λ to have optimum performance. The layout of the designed comparator is shown in Figure 4.10.

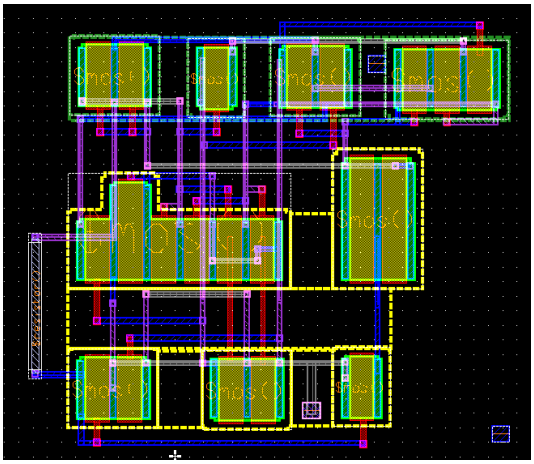

Figure 4.10: Layout of a comparator that has been designed

4.3. Result Summary

From the schematic simulation, the characteristic of the comparator that has been designed can be summarized as in Table 5.1

	Basic Comparator	**Comparator Designed**
Offset	14.04µV	620µV
Gain	7000	7147
High output level	4.97V	4.73V
Low output level	28.82mV	55.67mV
T_{pLH}	5.98nS	3.93ns
T_{pHL}	5.02nS	3.11ns
Propagation delay	5.5nS	3.52ns
Power consumption	0.908mV	0.9587mW

Table 5.1: Results show the characteristic of the comparator

5.0. CONCLUSION

The design of a comparator for 8-bit ADC in a 0.35µm CMOS technology based on the basic comparator architecture consisting of three stage that are pre-amp, decision circuit and output buffer. The combination of the pre-amplifier stage and a latch as the positive feedback decision circuit has successfully

brought the designed comparator to achieve good speed performance and very small offset voltage.

The ratio of the MOSFETs diffusion width to channel length (W/L) also contributes to the performance of the designed comparator. By simulation, it is found that the sensitivity of the comparator increases approximately in linear with increasing width of input MOSFETs (MN1 and MN2) in pre-amp stage while the offset voltage of the comparator is mainly determined by the width of MOSFET MN13 in decision stage. By setting the width of MN13 to 8λ, the comparator has achieved average offset voltage at 620µV.

The specified CMOS technology, the comparator is operated in supply voltage of 5V and resulting power consumption of 0.9587mW. As the designed comparator has relatively very high-sensitivity and close-to-zero offset, the faster time response is achieved although for small input voltage. The propagation delay is obtained at 3.52ns for difference input voltage of ±10mV.

6.0. FUTURE DEVELOPMENT

The designed comparator's gain and sensitivity can be increased by using larger width of MOSFETs MN1 and MN2 of the pre-amp stage. Another method to provide larger gain and higher sensitivity is by adding another gain stage to the pre-amp [7]. The continued drive toward technology scaling in VLSI design has provided greater integration levels in silicon chip. The feature size has been reduced year by year resulting lower power consumption with lower supply voltage.

The IC design of the comparator and the whole ADC can be implemented in low-power low-voltage technology by reducing the feature size. However, this development needs major modification to the designed circuit so that it can work in lower supply voltage.

7.0. ACKNOWLEDGEMENT

First of all, praise is only to Allah s.w.t for His bounty and blessing upon us who have give me strength and ability to complete this project and report. I would like to express my sincere appreciation to my supervisor, Puan Puteri Sarah Mohamad Saad for her opinion, guidance and invaluable advice upon completing this project. A very thankful was given to my parents who gives their loves and support for me directly or indirectly and to my entire friend for their time and support, giving ideas, comment and encouragement. This project wouldn't be possible without the helps from all of them.

8.0. REFERENCES

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