Zero Cross Detector Design Using Single Supply CMOS Operational Amplifier

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Abstract **- The purpose of this project is to explore the techniques in developing the low voltage CMOS analog building blocks such as operational amplifiers. The main objective of this project is to design the low voltage single supply CMOS operational amplifiers for zero cross detector application. Circuits were aimed to operate standard supply voltage (3V). Achievement of high gain around 80 dB and 45 degree phase margin for stable closed loop operations were the goal of primary concern for zero cross detector design. Designing, simulation and layout had been done. All the designs had been done using Tanner EDA with 0.25 µm technology where simulation had been carried out using SPICE simulator and layout had been made using Tanner layout editor (L-edit).**

Keyword-CMOS, operational amplifier, layout

I. INTRODUCTION

A. Operational Amplifier

Operational Amplifiers are one of the most widely used for analog systems. They are employed from dc bias applications to high speed amplifiers and filters. General purpose op amps can be used as buffers, summers, integrators, differentiators, comparators, negative impedance converters, and zero cross detector and many other applications. An operational amplifier is characterized by having two inputs, that is, an inverting or negative input and a non-inverting or positive input. The operational amplifier includes an output, that is, a single-ended amplifier, or two outputs, that is, a double-ended amplifier which is also known as a fully differential amplifier.

Two-stage operational amplifiers typically include a first gain stage connected to inputs of the amplifier and a second gain stage driven by the first gain stage. The second gain stage provides the output of the amplifier. Both the first gain stage and the second gain stage are operated at respective bias currents. In metal oxide semiconductor (MOS) amplifiers, the first gain stage is typically operated at bias currents which are comparable in magnitude to the bias currents of the second gain stage so that maximum gain and bandwidth may be achieved.

With the quick improvements of computer aided design (CAD) tools, advancements of semiconductor modeling, steady miniaturization of transistor scaling, and the progress of fabrication processes, the integrated circuit market is growing rapidly. Nowadays, complementary metal-oxide semiconductor (CMOS) technology has become dominant over bipolar technology for analog circuit design due to the industry trend of applying standard process technologies to implement analog circuits in chip. There has been a recent trend of placing digital or analog components on the IC chip for various applications.

B. Zero Cross Detector

A zero cross circuit define as an electrical circuit that starts operation with the AC load voltage at close to zero-phase. Zero-crossing detector delivers an output pulse that synchronizes other circuitry to the transitions through zero volts of a sinusoidal source for both polarity excursions. In operation, a zero crossing detector determine if an input voltage to the comparator is greater or less than zero .It used to convert sine wave or other signal into square-wave, the output should be low if the input is negative and high if the input if positive. The basic zero crossing detector can see on a single comparator as figure 1. An analog comparator has two inputs one is usually a constant reference voltage V_R and other is a time varying signal v_i and one output v_O. When the non inverting voltage is larger than the inverting voltage (Vr>Vi) the comparator produces a high output voltage ($+V_{sat}$). When the non-inverting output is less than the inverting input the output is low ($-V_{sat}$) as shows on figure 1.

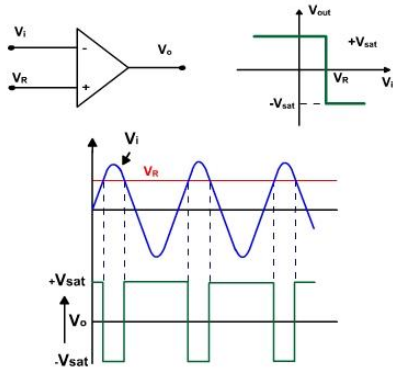

Figure 1 Zero crossing detector

For this purpose, the HI-8573 op amp was chosen. Its provide two-stage op-amp which its configuration has reasonably good quality in addition to the simplicity of circuit. Two stage op-amp configuration is composed of a differential amplifier input stage and a common source amplifier which is actively loaded by current source transistor. Differential

amplifier is used in first stage since they are less sensitive to noise as a result of high CMRR.

C. Layout

IC layout is the representations of an integrated circuit in terms of planar geometric shapes which correspond to the patterns of semiconductor layers that make up the components of the integrated circuit meet all criteria such as performance, size, and manufacturability.

The layout must pass a series of checks in a process known as verification. The two most common checks in the verification process are Design Rule Checking (DRC), and Layout Versus Schematic (LVS).

When all verification is complete the data is translated into an industry standard format and sent to a semiconductor foundry which converts the data into another format and uses it to generate the photomasks used in a photolithographic process of semiconductor device fabrication. Modern IC Layout is done with the aid of IC layout editor software, or even automatically using EDA tools, including place and route tools or schematic driven layout tools. For this purpose, the Tanner EDA tools were used.

II. METHODOLOGY

A. Schematic design

Two stage Operational Amplifier

The operational amplifier was designed follow the procedure below.

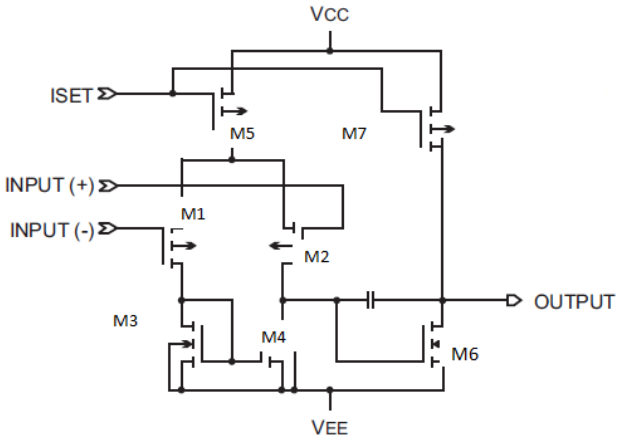

Figure 2 Two stage operational amplifier

$Si = \frac{Wi}{Li} = \frac{W}{L}$ of the *i*th transistor

This design procedure assumes that the gain at dc (*Av*), unity gain bandwidth (*GB*), input common mode range (*Vin*(min) and *Vin*(max)), load capacitance (*CL*), slew rate (*SR*), settling time (*Ts*), output voltage swing (*Vout*(max) and *Vout*(min)), and power dissipation (*Pdiss*) are given. The smallest device length which will keep the channel modulation parameter constant are chosen with current mirrors are given good matching.

-First, from the desired phase margin, the minimum value for *Cc* was chosen, i.e. for a 60° phase Margin, the following relationship was used. This assumes that $z \geq 10GB$.

$$Cc > 0.22CL$$

-Second, the minimum value for the "tail current" (*I*5) from the largest of the two values was determined.

$$I5 = SR\ .Cc \text{ or } I5 = 10\left(\frac{VDD+VSS}{2Ts}\right)$$

-Third, the value of *S*3 is determined from the maximum input voltage specification.

$$S3 = \frac{I5}{K'3[VDD - Vin(\max) - |VT03|(\max) + VT1(\min)]2}$$

-Forth, the pole of M3 was verified due to *Cgs*3 and *Cgs*4 (= 0.67W3L3*Cox*) will not be dominant with assuming it to be greater than 10 *GB*

$$\frac{gm3}{2Cgs3} > 10GB$$

-Fifth, *S*1 (*S*2) are designed to achieve the desired *GB*.

$$gm1 = GB.\ Cc \rightarrow S2 = \frac{gm2^2}{K'2I5}$$

-Sixth, *S*5 was designed from the minimum input voltage. First *VDS*5 (sat) was calculated then *S*5 is finding.

$$VDS5(\text{sat}) = Vin(\min) - VSS - \sqrt{\frac{I5}{\beta 1}} - VT1(\max) \geq 100\ \text{mV}$$

$$S5 = \frac{2I5}{K'5[VDS5(\text{sat})]2}$$

-Seventh, *S*6 was found by letting the second pole (*p*2) be equal to 2.2 times GB and assuming VSG4 = *VSG*6.

$$gm6 = 2.2gm2(CL/Cc) \rightarrow S6 = S4\frac{gm6}{gm4}$$

*I*6 was calculated from

$$I6 = \frac{gm62}{2K'6S6}$$

It was checked to make sure *S*6 satisfies the *Vout*(max) requirement.

-Eighth, *S*7 was designed to achieve the desired current ratios between *I*5 and *I*6.

$$S7 = (I6/I5)S5$$

(The minimum output voltage requirements was checked)

-Ninth, the gain and power dissipation specifications were checked.

$$Av = \frac{2gm2gm6}{I5(\lambda 2 + \lambda 3)I6(\lambda 6 + \lambda 7)}$$

$$Pdiss = (I5 + I6)(VDD + |VSS|)$$

If the gain specification is not met, then the currents, *I*5 and *I*6, can be decreased or the W/L ratios of M2 and/or M6 increased. The previous calculations must be rechecked to insure that they are satisfied. If the power dissipation is too high, then one can only reduce the currents *I*5 and *I*6. Reduction of currents will probably necessitate increase of some of the W/L ratios in order to satisfy input and output swings.

The circuit was simulated using Tanner TSPICE to check that all specifications are met. The AC analysis was performed on the designed operational amplifier circuit to obtain the magnitude and phase plots. The DC power dissipation and output-offset voltage were obtained by performing operating point analysis on the circuit.

Zero Cross Detector

The op amp that was fulfills the requirement for zero cross detection then applied on zero cross detector circuit. The zero cross detector was designed to convert a low amplitude signal into a clean square wave signal. It can work with input as small as 5mV peak-to-peak or as large as 3 volts peak to peak. The input frequency can range from a few kilohertz to about 150kHz.

TSPICE transient analysis was used to obtain the square-wave output, which the output should be low if the input is negative and high if the input is positive. The obtain output match with the expected output prove the circuit was function and it enable to continue for the layout design.

B. Physical Layout Design

The layout of the designed was done in L-Edit Tanner software. L-Edit is a complete integrated circuit (IC) layout editor with many built-in tools including a design rule checker and a layout extractor which gives designers complete control over of layout operation.

Capacitor Layout

The op amp schematic involve capacitor component, so the layout of capacitor need to create and extract first. In principle, capacitor is nothing but two adjacent conductor plates with certain type of dielectric in-between. Therefore, the exact structure needs to know before drawing the layout in L-Edit. This structure was calculated based on the following formula:

$$Area\,(\mu m2) = \frac{capacitor\ value\,(F)}{capacitor\ per\ unit\ area\ (fF/\mu m2)}$$

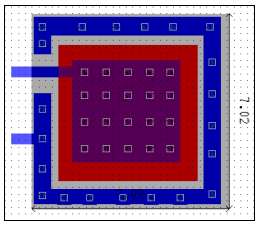

Figure 3 Capacitor layout

Resistor layout

Integrated resistors can be made by different layers (diffusion, well, poly). In analog applications linear resistors are usually required, so that they are typically implemented using poly. The design of resistor layout using the basic formula as below:

$$LW = \frac{resistor\ value}{resistor\ per\ unit\ area\ (\Omega/\mu m2)}$$

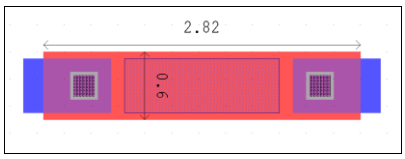

Figure 4 Resistor layout

Operational Amplifier Layout

Before produce the intend layout, the oriented layout was design first. Then the layout design need to confirm to a set of layout design rules, which dictate the geometrical constraints imposed upon the mask layers by the technology and by the fabrication process. The layout design rules may still result in a functional chip, but the yield is expected to be lower because of random process variations. This is where an LVS check is used. LVS checking software recognizes the drawn shapes of the layout that represent the electrical components of the circuit, as well as the connections between them.

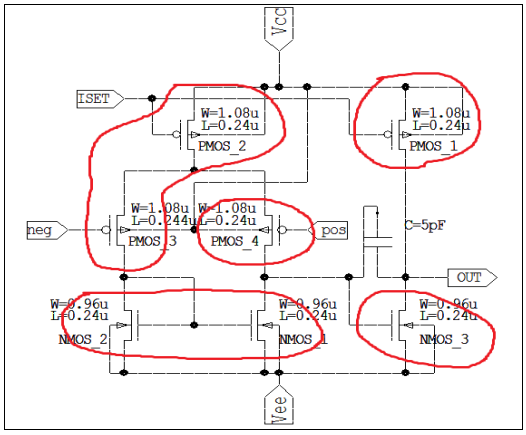

Figure 5 Op amp layout oriented

Zero cross detector layout

The mask layout designs of zero crossing detectors follow the general principles examined earlier for the CMOS op amp. The previously designed op amp, resistor and capacitor had been inserted refer to zero cross detector circuit.

III. RESULT AND DISCUSSION

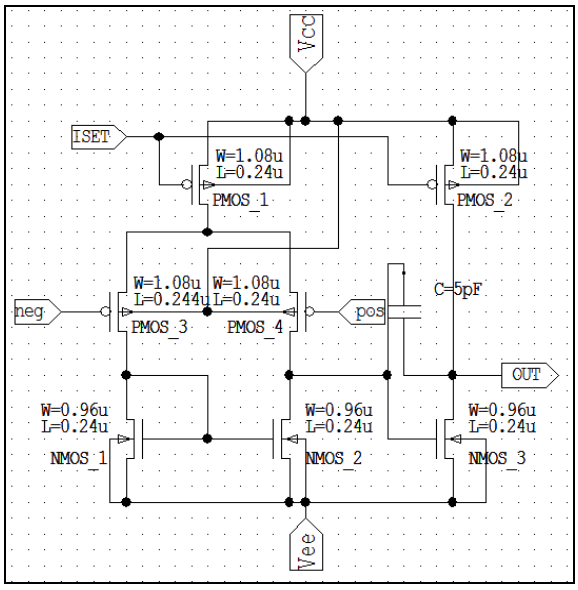

Figure 6 Two stage operational amplifier schematic

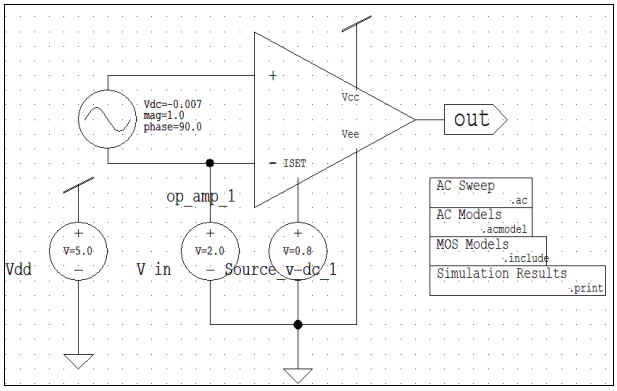

Figure 7 Ac analysis of two-stage op-amp

As seen in Fig.7 output point of two stage op amp is biased around 0.8V in order to have proportional voltage headroom and legroom. Thus it is prevented to lead a situation like high voltage headroom with low legroom or vice versa.

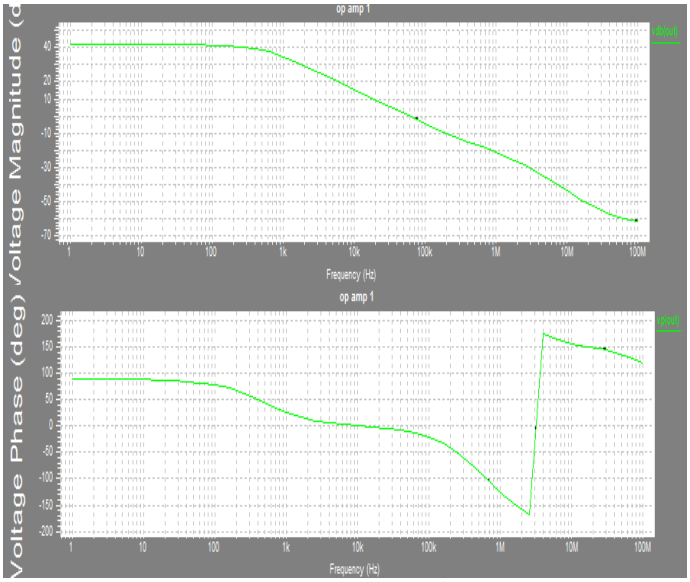

Figure 8 Frequency response of op amp

As seen in Fig.8 DC gain of two stage op amp is 40dB which is lower than the value in datasheet. Distinction between in the datasheet and simulation may be derive from some assumptions we made and Tanner also takes account of higher order effects of transistors during simulations. Also the unity gain frequency of op amp is 0.1MHz according to Fig8 lower than the value from datasheet (1.4MHz). In addition, in Fig.14 we get PM around 80degree, higher than the datasheet value (~45).

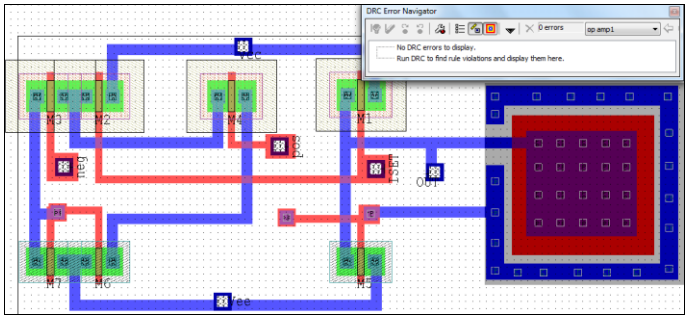

Figure 9 Results of DRC simulation of two-stage op-amp

In order to design layout in as minimum area as possible, almost after each connection, DRC used to determine if connection violate a design rule or whether it is possible to use connection closer to other component or not. Thus, at the end of layout design there no DRC error faced as seen in Fig. 9.

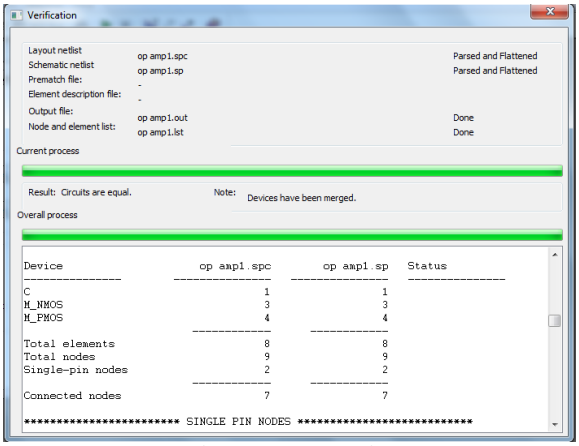

Figure 10 Result of LVS Simulation of Two-stage op-amp

As seen in Fig.10, layout and schematic of two-stage op amp in Fig.6 is matched at the end design. However, they were not matched in the first attempt since bodies of all nmos transistors in layout and schematic did not matched each other. In order to resolve this problem, more PDC contacts are used such that all nmos transistors are close to contacts.

After DRC and LVS simulations, op amp layout result like follow:

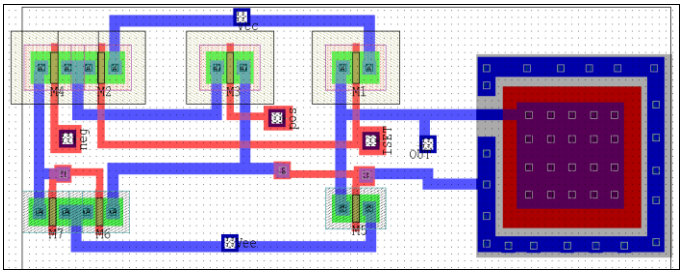

Figure 11 Layout level design of Two-stage op-amp.

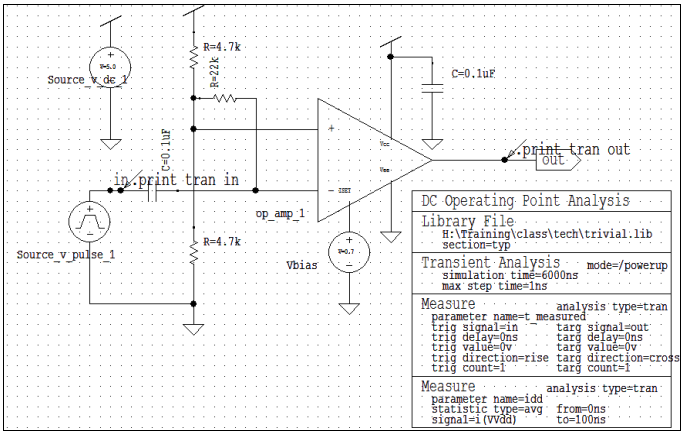

Figure 12 DC operating point of zero cross detector

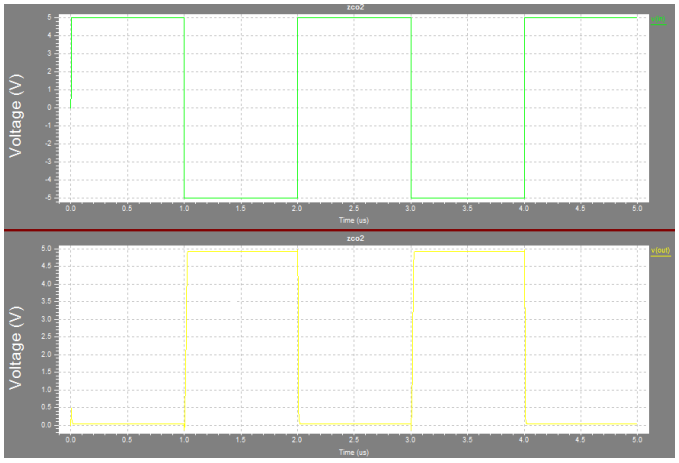

Figure 13 Zero cross detector transient analysis.

As seen in figure 13, the dc output of zero cross detector circuit was match with the expected output prove the circuit was function and it enable to continue for the layout design. The square-wave output show the output was low when the input is negative and high when the input is positive.

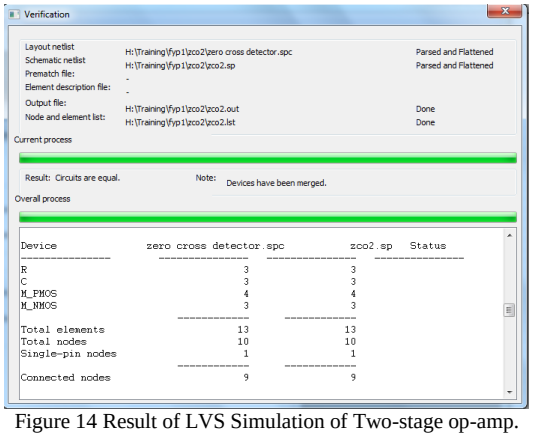

Figure 14 Result of LVS Simulation of Two-stage op-amp.

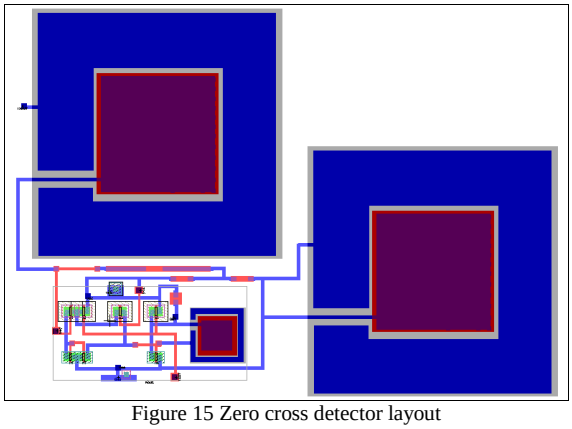

Figure 15 Zero cross detector layout

As seen in figure 14, the extracted layout net list show the netlist of layout and schematic were match, which means the circuit passes the LVS check. Actually it takes time for passes the LVS check where there errors that make the netlist mismatch. The errors that have been identified while troubleshooting includes the wires short, component mismatches or missing, and the wires or components that should be connected are only partially connected. The completed zero cross detector layout are shown in figure 15.

IV. CONCLUSION

The design and simulation of two stage operational amplifier and its application on zero cross detector has been proposed and discussed in this thesis. The electrical characteristics of the amplifier were obtained. The presented operational amplifier have successfully demonstrated that can applied as zero cross detector. The layout passes the LVS check which means the layout was represent the electrical components of the circuit, as well as the connections between them and match with schematic.

The layouts that have designed series with recommended by tanner but it not fulfill the requirement for layout fabrication because there no option for parasitic extraction. Parasitic extraction needed to ensure the design function within specification. It is important for standard IC verification due to performance, accuracy and reliability. In running this, its need the HiPER Verify from Tanner that not provided. The missing of this option unable to meet the requirement of IC standard verification that make the layout only applicable for learning process.

V. RECOMMENDATION

In general, most of the circuits that are included in this paper operated as intended. In some cases, revised designs such as amplifier were able to achieve higher gain and greater stability when simulated using the updated process parameters.

At the conclusion of this project, it became evident that the size of this circuit surpassed the capability of the design tools. T-Spice was able to effectively simulate the individual parts of the design, but it was only able to provide a rudimentary idea of the output of the completed operational amplifier.

It is interesting to note that different versions of the simulation tool produced strikingly dissimilar results. For example, an amplifier that may have achieved 60db of gain in an old simulation engine may only yield 40db of gain using a later simulation engine. Consequently it is recommended that in the future, the following changes be made to the simulation approach:

• *Use different design/simulation tools*. As previously explained, it has been found that the circuit design tools are not able to effectively simulate a circuit of this complexity. Therefore, I suggest that the circuit be simulated with another tool that is able to produce consistent results.

• *Re-simulate the op amp and zero cross detector using different constraints.* That is to say, that design should be re-simulated by driving the circuit with a various signal. While the DC analysis seems to indicate that the circuit is working properly, it would be advisable to confirm this using another type of simulation.

Since the layouts that have designed not fulfill the requirement for layout fabrication because there no option for parasitic extraction which important for standard IC verification. So, to ensure that this layout can be implemented for fabrication, this design can be improvise by adding HiPER Verify option on tanner or using the advance and updated software such as mentor design and cadence software. Actually the tanner that provided by UiTM just only for the learning purpose, not for industry fabrication.

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