A Low Frequency of Planar Diplexer Based On The Substrate Integrated Waveguide (SIW) Technology with Circular Cavity

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***Abstract*— This paper presents the prototype design of S-band diplexer using Substrate Integrated Waveguide Technology (SIW) with circular cavity. The diplexer will operate at S-band frequencies which related to the mobile tv and satellite radio application. SIW technology and circular cavity is used to design the diplexer due to its attractive advantage of reduction in size and low cost. The simulation has been performed by using CST Microwave Studio.**

Keywords—substrate integrated waveguide (SIW), diplexer, microstrip, S-band, circular cavity

I. INTRODUCTION

A diplexer is a combination of filters with the same common feed point. It is used for signals separation travelling from one input port to multiple different paths [1]. Systems performance is depending on the diplexer at the transceiver end which can give great impact on the channel separator [2]. Diplexer design is usually based on waveguide technology with excellent performance in terms of insertion loss and channel-to-channel isolation. However, it is impossible to integrated with the rest of the millimeter-wave planar integrated circuits that has the transceiver front end [1-3]. The design also suffers disadvantages such as being bulky, costly, and difficult to fabricate. Thus, the implementation of SIW technology is the best candidate to resolve the mentioned disadvantages.

II. SUBSTRATE INTEGRATED WAVEGUIDE & DIPLEXER

Metallic waveguides are basically a device for transporting electromagnetic energy from one region to another. Typically, waveguides are hollow metal tube (often rectangular or circular in cross section) [7]. Physical size is the primary lower-frequency limitation of waveguides. The waveguides that is designed for lower microwave frequencies tend to be larger and bulkier. This technology is often more expensive due to the higher cost of waveguide materials, such as silver and copper [8].

A substrate integrated waveguide (SIW) is chose for this prototype. A waveguide or its cavity, when it is integrated into the substrate-based circuit and the propagating waves are constrained by arrays of via holes, is then referred to as a SIW [5]. In the structure of SIW filters, the fence of 'via' holes which connected circularly between the top and bottom conductors will form a cavity wall, wherein the microstrip transmission line is used as the input and the output feedline [3]. As shown in figure 1, these cavity walls consisting of rows via will provide out-of-band rejection, making it suitable for use in S-band applications.

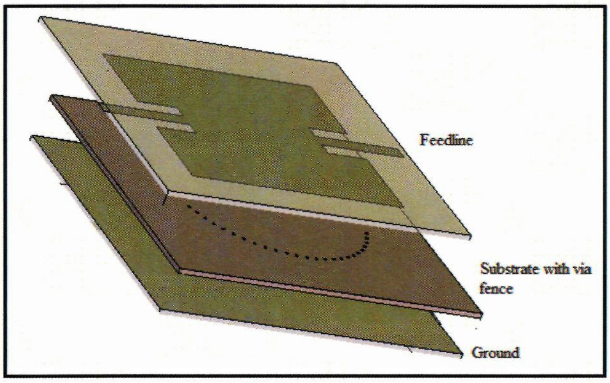

Figure 1. Basic configuration of SIW structure

A diplexer is used to route signals to two different receivers, based on the frequencies. Diplexers can use low-pass, high-pass or band-pass filters to achieve the desired result. [6] The simplest way to implement a diplexer is to use a low pass and a high pass filter. In such way, the diplexer will routes all signals at frequencies below the cut-off frequency of the low pass filter to one port, and all signals above the cut-off frequency of the high pass filter to the other port.

The ports of a diplexer are frequency selective, which makes it different from a passive combiner or splitter. Ideally, the separation of the signals is complete. But in the real world, some power will be lost, and some signal power will leak to the wrong port [7-8].

III. METHODOLOGY

This project started with background studies about diplexer and SIW. SIW diplexer is designed by using CST started with single order and followed by first order. After simulation, the obtained result is discussed. The design will be re-simulate if there is any adjustment/optimization being made. The project is finish once the design reached its designated results. Figure 3 shows the flow chart of the project.

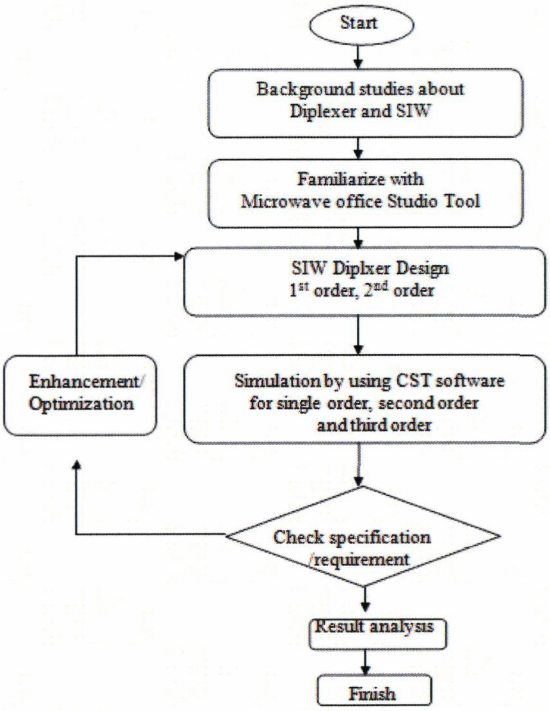

Figure 3. Flow chart of the project

The available substrate in lab is Rodgers RT/duroid with Er = 2.2. The substrate can be at any thickness since it does not affect the cut off frequency [12]. As shown in figure 1, the available diameter of via hole **‘D’** in lab is 1 mm with PEC material. To ensure lower leakage loss between adjacent posts, the pacing between the holes **‘b’** must be kept small. In [7] and [12], had demonstrated two design rules related to the post diameter and pitch used to ensure that the radiation loss is kept at a negligible level, formulated as below;

$$D < \frac{\lambda_g}{5} \tag{1}$$

$$b \leq 2D \tag{2}$$

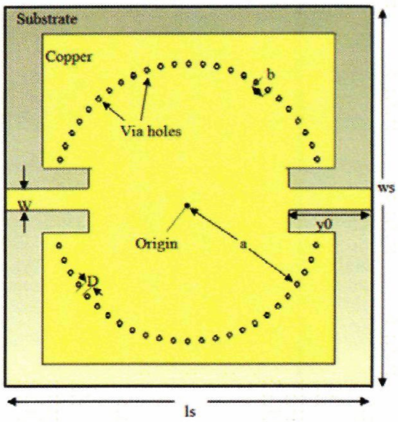

Figure 2. Single Order SIW structure

The design started with single order by calculating the radius from origin to the via holes **‘a’** operate at frequency of 2.1GHz and 2.7GHz respectively, as shown in figure 2. TMmn modes is used because these modes exist only in circular substrate integrated waveguide. TM_{010} is considered to be the dominant mode for circular waveguide and has a single mode resonator [5].

With TM_{010} mode, **‘a’** can be obtained by using the formula below[12]:

$$(f_r)^{TM^z}_{mnp} = \frac{1}{2\pi\sqrt{\mu\varepsilon}}\sqrt{\left(\frac{\chi_{mn}}{a}\right)^2 + \left(\frac{p\pi}{h}\right)^2} \qquad \begin{matrix} m = 0,1,2,3,... \\ n = 1,2,3,4,... \\ p = 0,1,2,3,... \end{matrix} \tag{3}$$

For the first order, the channel filter is being cascaded with 2 circular cavities in the designated substrate as shown in Figure 4 and figure 5. Port 1 is fed to microstrip. Port 2 is connected to 2.7GHz and port 3 is connected to 2.1GHz.

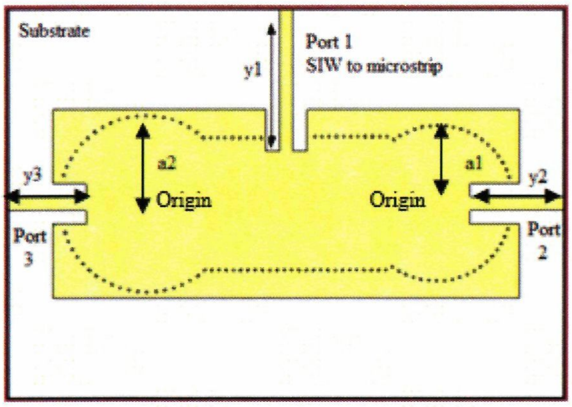

Figure 4. First Order SIW structure

The inset method is used to act as the input port of the diplexer. The depth of inset excitation structure (y1, y2, y3) is being optimized accordingly until the 50Ω transmission line impedance matches the input impedance of the SIW resonator. The width (w) of the inset feeding is set to be similar to the width of the transmission line. This is the simplest approach to determine the dimension of the transition between microstrip line and circular SIW resonator. The SIW designed parameter is as tabulated in Table 1.

TABLE I. SIW DIPLEXER DESIGNED PARAMETER AT S-BAND FREQUENCIES

Parameter	*Symbol*	*Value*	*Unit*
Dielectric substrate	RT/Duroid 8880 (ε_r = 2.2; h = 1.57)		
Pitch via	b	6	degree
Via diameter	D	1	mm
Microstrip feed width	w	4.878	mm
Substrate length	ls	240	mm
Substrate width	ws	140	mm

Parameter	*Symbol*	*Value*	*Unit*
Inset at port 1	y1	15	mm
Inset at port 2	y2	14	mm
Inset at port 3	y3	12	mm
Diameter at 2.7GHz	a1	28.7	mm
Diameter at 2.1GHz	a2	31	Mm

IV. RESULT AND ANALYSIS

Figure 5 and figure 6 are the results for single order of 2.1GHz and 2.7GHz respectively.

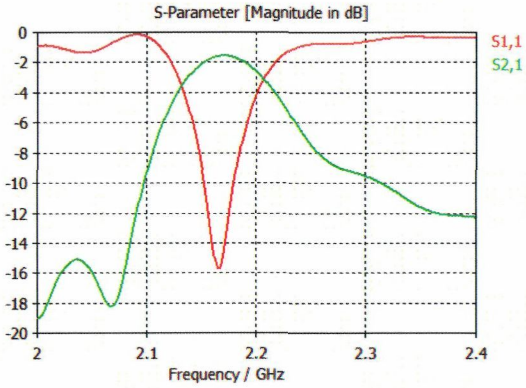

Figure 5. S-parameter for 2.1GHz

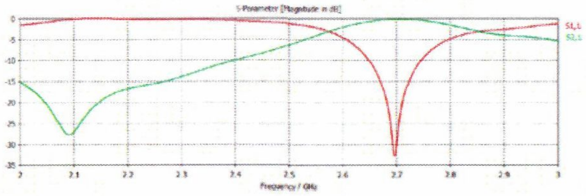

Figure 6. S-parameter for 2.7GHz

For the first order SIW diplexer design, the parameter used for lower channel filter are y_3=14mm, a = 31mm. For higher channel filter, the parameter used are y_2=14mm, a = 28.7mm. Figure 7 shows the return loss (S_{11}) at the common port of the diplexer. It varies below 10dB in the passband. The bandwidth at the high channel is 51MHz and at the low channel is 26MHz.

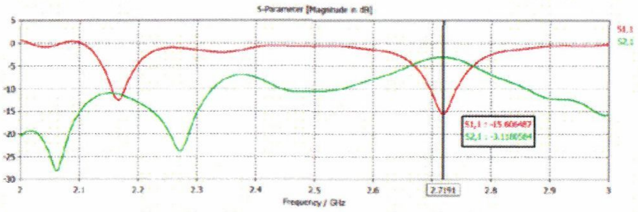

Figure 8. S-parameter for higher channel

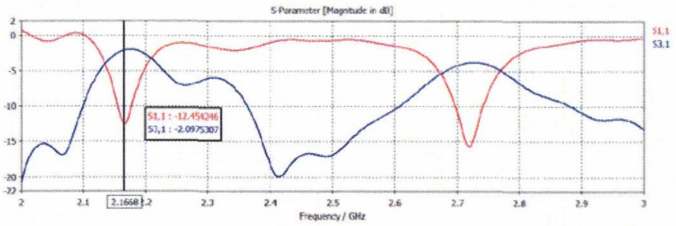

Figure 9. S-parameter for lower channel

Figure 9 and figure 10 shows the electric field at port 2 and port 3 respectively. This result clearly support that the SIW diplexer can be construct. Therefore, there is a lot of adjustment and optimizations need to be made for a better result.

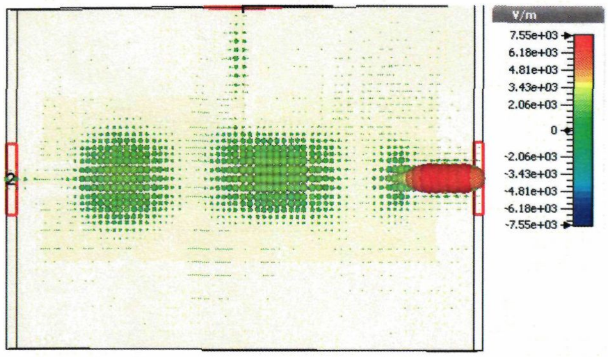

Figure 9. E-field from port 3

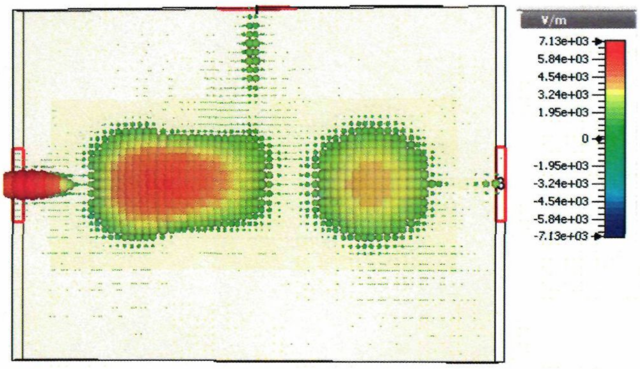

Figure 10. E-field from port 2

V. CONCLUSION

An effort has been made to design the prototype of low frequency of planar diplexer based on the substrate integrated waveguide (SIW) technology with circular cavity. Simulation result has shown that by using the SIW technology with circular cavity can reduce the size of the diplexer. The wave propagation via inset method as the feedline to microstrip also shows some reflected signals at the port area. Therefore, a technique such as tapper or T junction can be another option for a better result.

VI. REFERENCE

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