# Simulation of Planar and FinFET Transistor Model for Digital Gate Applications

Siti Aishah binti Abu Salim
Faculty of Electrical Engineering
Universiti Teknologi MARA Malaysia
40450 Shah Alam, Selangor, Malaysia
*caa_ee@yahoo.com*

*Abstract* –**In this work, FinFET (dual-gate) transistor is simulated using computer added design (CAD) tools to replace the conventional planar MOSFET. Nowadays planar transistors are no longer clean due to current leakage during on-off switches. Thus, these effects have caused some heat and power issues. FinFET transistors offer superior performance as the device is scaled into the nanometer. Therefore, the ON current was investigated by analysing the *I-V* characteristic. Also the gate sizing was investigated and the results have shown the differences in their performances. In addition, the SPICE models of 32 nm were employed for inverter, NAND and NOR gates and the results were verified by DC and AC analysis. The results indicate that FinFET circuits have better performance and produced less leakage when compared to planar MOSFET.**

***Keywords – Planar MOSFET, Double-gate FinFET***

## I. INTRODUCTION

Moore's Law states that the density of transistor and performance of chip will double approximately every two years [1]. Generally, a planar transistor consists of source, drain, gate, and channel. The channel connects the source and drain whilst the gate placed top off. From the past few decades, to improve the performance of the transistors the chip makers shrink the device into two-dimensional or planar structure.

However, the problem that the chip makers faced was it is difficult for the transistor to turn off when the size is smaller [2].Therefore, in a continuous effort to improve the device, the structure was transferred from planar to three-dimensional device. FinFET device promise to replace planar MOSFET because of the ability in minimize the short channel effect and in control leakage. Generally, FinFET have the same feature with planar transistor that consist of source, drain, gate and channel. The difference is that FinFET has a thin and a vertical strip of silicon called fin, located between the source and drain. At the ends of the fin, two polysilicon electrodes contacted along the vertical sides of the fin located between the source and drain. Typical thicknesses of the fin is in the range of 10 nm to 50 nm, while the height of the fin was equal to or larger than the channel width, e.g. 50 nm[3].

FinFETs are double-gate devices [4]. The two gates of a FinFET can either be shorted for higher perfomance or independently controlled forlower leakage or reduced transistor count. This gives rise to a rich design space.

In this work, comparison between planar MOSFET and FinFET transistor will be investigated. The performances of both transistors will be examined using CAD tools where the model is verified by simulation into *LTSpice* simulator. By using *LTSpice*, the *I-V* characteristic can be defined.The architecture of the device will be performed using *Microwind*. The parameter that to be analyzed: gate length. The SPICE models were verified by DC analysis of inverter. Lastly, the simulations of digital gate will examine using both SPICE models.

## II. METHODOLOGY

In this project, the comparison was made using CAD tools: Three-dimensional view and SPICE simulator. Fig. 1 depicts the flow chart of the overall project design.

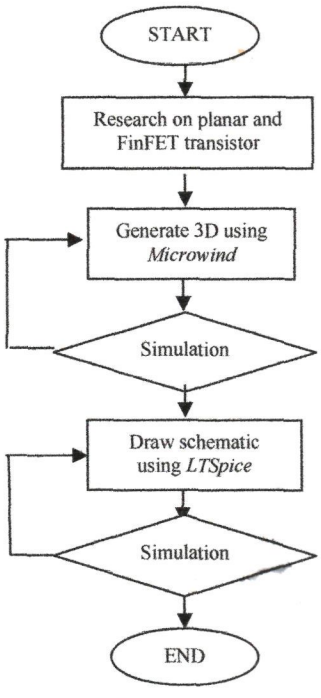



**Fig. 1**: Flow chart of design

The project starts with research about planar and FinFET transistor. It is understood that FinFET is an improvement of planar transistor. Both devices will be examined with structural variation and their effect on their performances.

The 3D view this project is to provide a simulation of MOSFET and FinFET transistor and identify the behavior of both transistors. *Microwind*is used to get the 3D view of the transistor. The software has a generator as shown in Fig. 2 for MOSFET and FinFET (dual-gate) transistor respectively and then 3D structure were simulated.

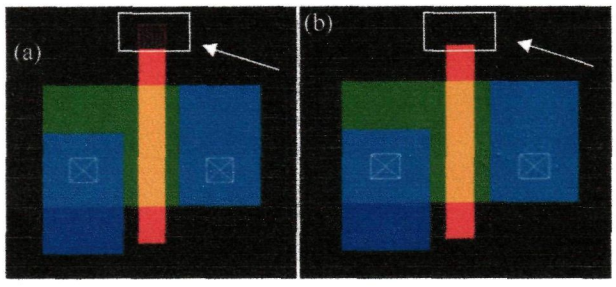
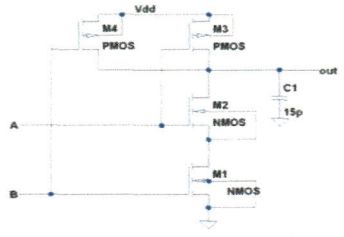



Fig. 2: Layout of generator MOSFET (a) and FinFET (b) that different at the gate

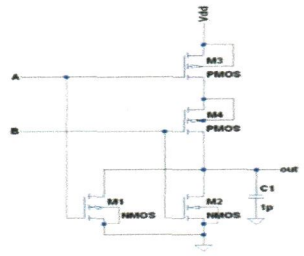
In the simulation work, both MOSFET and FinFET schematic diagram is requiredin order to represent the *I-V* characteristics of transistor. The transistors were simulated using *LTSpice*. In the *LTSpice*, there's no symbol for FinFET. Thus, SPICE models were employed to obtain accurate model for each devices. The models are available at ptm [5] site by using the same MOS symbol, Fig. 3.


Fig. 3: MOS symbol

Then, the verifying models were done to identify whether the model matched the operation well. Lastly, the application comparison using NAND and NOR gates of both model. Fig. 4 (a) and (b) shows the schematic diagram for NAND and NOR. Both MOSFET and FinFET used the same schematic but different SPICE model.




(a)




(b)

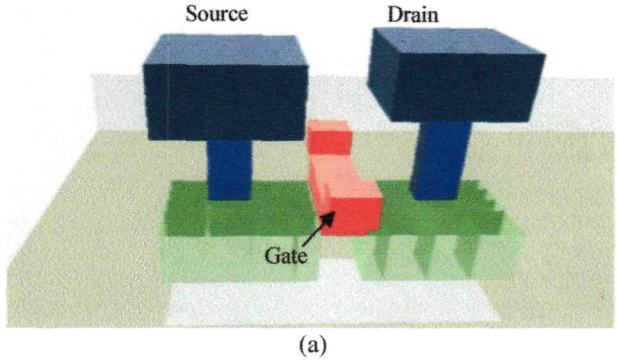
Fig. 4: Schematic diagram of (a) NAND and (b) NOR

## III. RESULT AND DISCUSSION

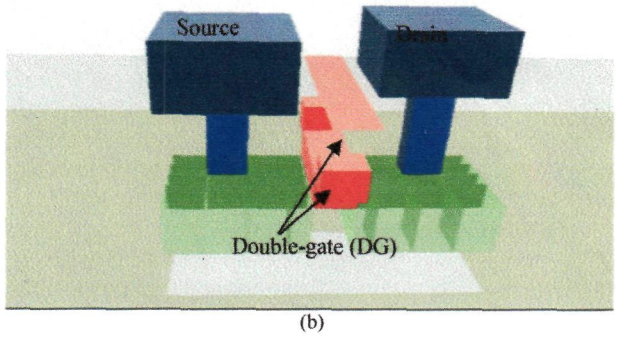
The following section is divided into 3 parts. Part A: 3D view and comparison of *I-V* characteristics, while Part B is the verification of the model using DC analysis. Digital Gate application using MOSFET and FinFET models in Part C.

### *A. 3D View And Comparison of I-V Characteristics*

The simulation results of both devices were presented according to *LTSpice* and *Microwind* simulator. Both devices were compared based on the performance of MOSFET and FinFET transistor. Fig. 5 (a) and (b) presents the 3D views of MOSFET and FinFET transistor and its *I-V* curve respectively using *Microwind* simulator. Basically, FinFET have the same feature with planar transistor that consist of source, drain, gate and channel. The different between MOSFET and FinFET is FinFET has double gate.



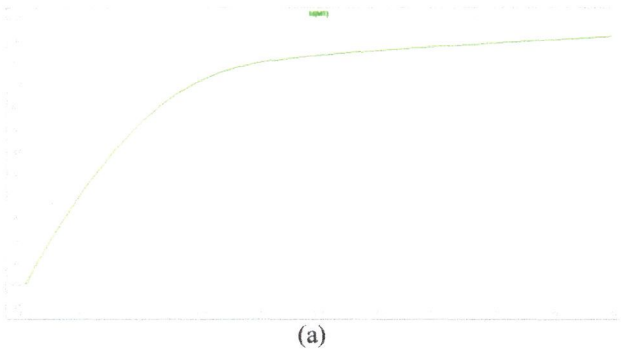

(a)



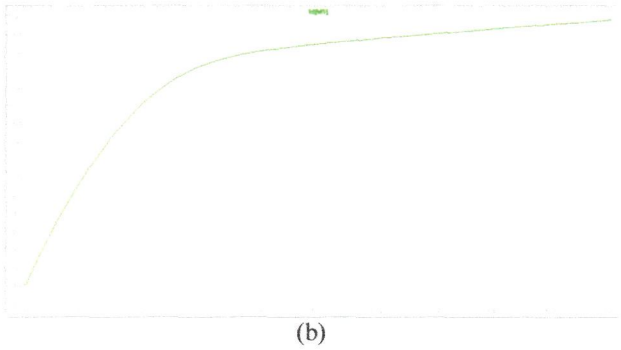

(b)

Fig. 5: 3D view of (a) planar MOSFET and (b) Dual-gate FinFET transistor

From the Fig. 5 it is shown that FinFET have two gates while MOSFET has only one gate between the drain and source. With two gates the current can be easily switched ON-OFF. The two gates have better ability to turn off the gate which for allows modulating the channel from two sides instead of one [6].



(a)



(b)

Fig. 6: *I-V* curve of (a) planar MOSFET and (b) Dual-gate FinFET transistor

Another simulation was performed using *LTSpice* with *SPICE* model of 32 nm technology referred to Ref. [5]. Based on the Fig. 6 the *I-V* curve, the ON current, $I_{ON}$ for MOSFET around 34.5uA while FinFET around 14.8uA. This shows that FinFET transistor has smaller $I_{ON}$ compared to MOSFET. Thus, this implies that FinFET is easily turned off and leakages current reduced [6].

The devices were assumed to have the initial gate length and a body width of 50nm each. The gate length was varied to investigate its effect of on device behavior.

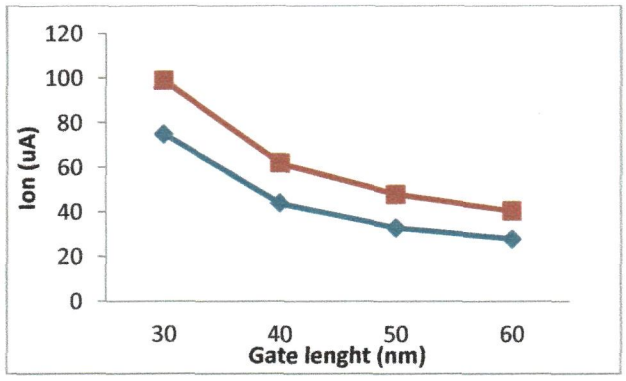
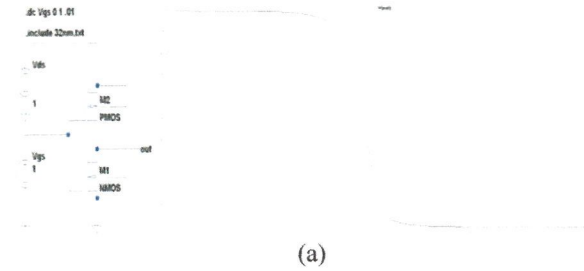



Fig. 7: $I_{dsat}$ for a MOSFET ( ■ ) and a FinFET ( ◆ ) for variation in length of gate.

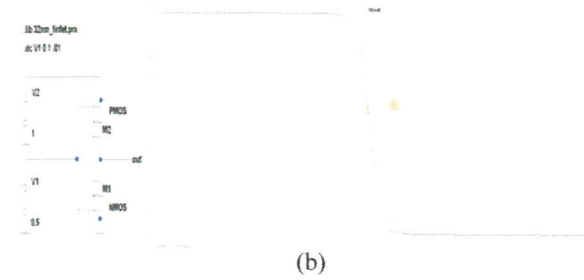
As shown in Fig. 7, the variation of gate length with constant gate width of 50nm. The increasing of $I_{ON}$ depends on decreasing of gate length. If the gate length of the transistor was smaller, the gate's control over the transistor had gotten weaker since the distance between source and drain were getting shrunk [7]. The double-gate FinFET transistor offers better performance as gate length scale below 60nm compared to planar MOSFET transistor.

### *B. Verification of the model using Inverter*

DC analysis of the inverters using MOSFET and FinFETs SPICE model was done and are compared for the noise margin parameters. The input output waveforms of the inverter using MOSFET and FinFETs are shown in Fig. 8, respectively. The back-gate of the devices in the inverter is to set the different voltages and 1V power voltage was applied.



(a)



(b)

Fig. 8: DC characteristics of an inverter (a) MOSFET and (b)FinFET

The different input, output voltage levels required for noise margin calculation are tabulated in Table 1 for MOSFET and FinFET. There is small drop in the noise margin of the inverter if FinFETs are used.

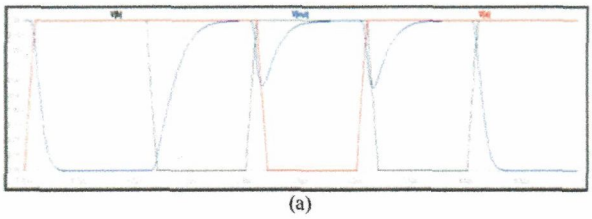
Table 1: DC analysis of Inverter using MOSFET and FinFET

| Voltage level | MOSFET | FinFET |
|---|---|---|
| $V_{OH}$ (V) | 0.93 | 0.97 |
| $V_{OL}$ (V) | 0.05 | 0.04 |
| $V_{IH}$ (V) | 0.51 | 0.53 |
| $V_{IL}$ (V) | 0.39 | 0.45 |

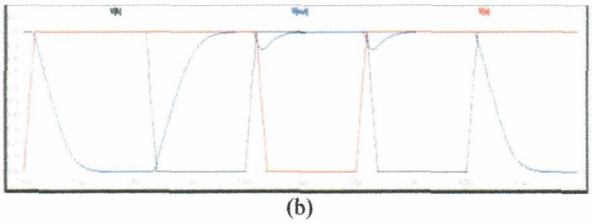
The results revealed that FinFET transistor drop directly when the gate voltage turns to zero. This resulting in faster switching times. This shows that MOSFET takes much time when the switch is turn off. It can be seen that using FinFET leakage current will reduce because no power excess during turning off.

### C. *Digital Gate Application using MOSFET and FinFET models*

In previous section, it is observed that double-gate FinFET has lower leakage current and offer several advantages over planar MOSFET. In this section, both SPICE models were used for the simulations of digital gate such as NAND and NOR are compared for the delay. Figs. 9and 10 showed the transient input and output for NAND and NOR gates using MOSFET and FinFET respectively. It is seen that the model matched well almost in all operations.

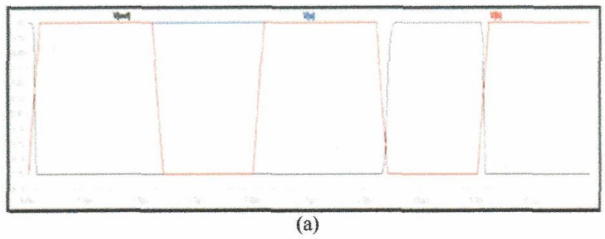


(a)

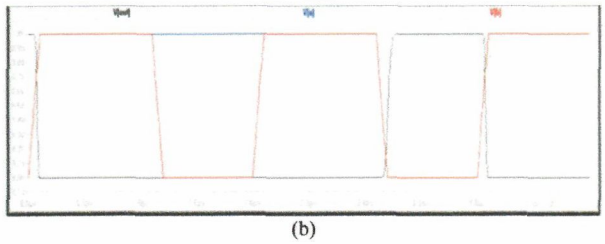


(b)

Fig. 9: Transient NAND of (a) MOSFET and (b) FinFET



(a)



(b)

Fig. 10: Transient NOR of (a) MOSFET and (b) FinFET

Table 2: Delay parameters for CMOS Inverter using MOSFET and FinFET

| **Gates** | **Delay parameter** | MOSFET (**µS**) | FinFET(µS) |
|---|---|---|---|
| **NAND** | $t_{pdr}$ | 0.250 | 0.187 |
| | $t_{pdf}$ | 0.118 | 0.118 |
| **NOR** | $t_{pdr}$ | 0.075 | 0.062 |
| | $t_{pdf}$ | 0.000 | 0.031 |

The propagation delay of the respective NAND and NOR gates are tabulated in Table 2, which show that the gates with MOSFET had larger delays compared to the gates with FinFET. Thus, switching is faster with design of FinFET. This is due to the conductive path that created when the gate turned on to allow the electrons and holes moves from drain to source [8] was disappear immediately when the gate was turned off.

## IV. CONCLUSION

In conclusion, we have compared planar MOSFET and three-dimensional FinFET device characteristics and the performance of digital circuits designed with those devices. For three-dimension FinFET (dual-gate) transistor has better performance compared to planar transistor. Since the leakage current of FinFET transistor is lower, the transistor is easily turn OFF-ON. It is seen that the model matched well almost in digital gate application. There is small drop in the noise margin of the inverter if FinFETs are used. The NAND and NOR has been taken as an application circuit which shows that FinFET offers lower delay compare to MOSFET because the capacitance is reduced [9].


## ACKNOWLEDGMENT

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