The Phase-Change Memory with a Separate-Heater Layer Design for The Multilevel Storage Device

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Abstract- A phase-change memory structure with a separate heater layer was proposed to perform a multilevel storage. This is to overcome the problem faced by the conventional design which is the difficulties to control the crystallization process in order to achieve the multilevel storage. A finite element analysis was conducted to investigate the possibility of multilevel storage using COMSOL 4.4 software. A 100ns SET pulses with an increasing amplitude from 0.1V to 0.7V were applied for heating the memory layer, which is $Ge_2Se_2T_5$ (GST). The transition from the amorphous to the crystalline phases induced by heating the material above its crystallization temperature (450K-900K) and switching back to the amorphous state is realized by melting and quenching the material. The result is the proposed design shows more data to be stored in order to achieve the multilevel storage than the conventional design of phase-change memory with a 50nm thickness of memory layer (GST) and the 500nm width of the structure itself.

Keywords-component: phase-change memory, separate heater layer, multilevel storage, crystallization process, nonvolatile memory

I. INTRODUCTION

A phase-change memory (PCM) is one of the candidates for the next technology of nonvolatile memory [1-3]. There are many advantages of PCM over the flash memory that we are using right now; it has low programmable energy, high endurance, fast switching speed, good data retention, improved compatibility with complementary metal oxide semiconductor (CMOS) and excellent scalability [4]. The chalcogenide glasses is used as the phase-change material that possesses highly different electrical resistivity depending on its phase. Resistance will be high when it is in amorphous phases and it will be low when it is in crystalline phases [5-6]. The intermediate resistance levels are expected to be more between these two phases to allow the multilevel storage memory.

When the SET (crystallization) pulse is directly apply to the two sides of the chalcogenide layer, sudden change will occur [7]. It shows that it is difficult to control the crystallization process in conventional phase-change memory device.

In order to solve the problem, the proposed design of phase-change memory with a constant resistance separate heater layer is used to gain the multilevel storage. The insulator will be added between the heater and the memory layer to ensure that resistance can be control well and to prevent the electrical contact between heater and the memory layer. The capping layer also will be used to prevent the thermal loss from heater layer to the surrounding [8].

II. METHODOLOGY

The phase-change memory device structure is analyzed by using COMSOL 4.4 software which is 3D illustration. The roughly design with random parameters of structure measurement is sketched before be implemented into the software. After that, the result will be simulated to find the best material and parameter of the structure that allow the most efficient multilevel storage. The material properties that have been used for both conventional and proposed design of the phase-change memory is shown in Table 1.

Table 1: Physical Properties of Materials Used in the Simulation

Material	Heat Capacity (C) j/(kg*K)	Thermal Conductivity (K) W/(m*K)	Density (ρ) Kg/m^3	Electrical Conductivity (σ) S/m
SiO_2	1330	1.4	2330	1.0 x 10^{-14}
TiN	784	22	5240	5.0 x 10^{6}
GST	202	0.46	6200	3.6 x 10^{-1}
ZnS-SiO_2	263	0.657	3650	0.02

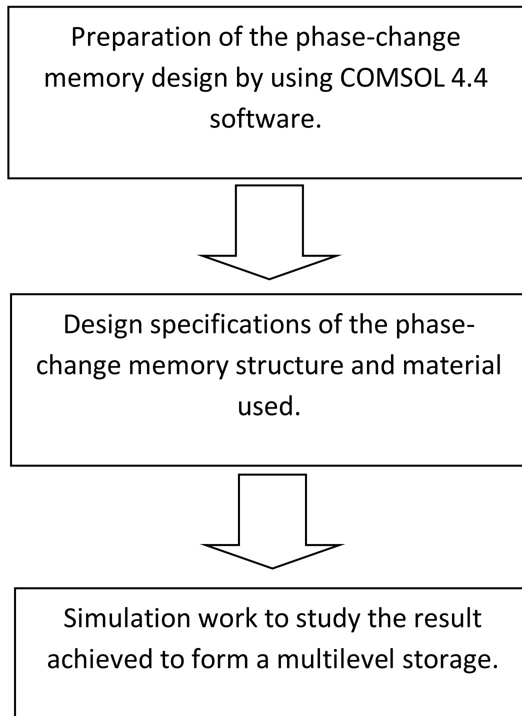


Figure 1: Design Flow for the Simulation

Figure 1 shows the design flow for both conventional and the proposed designs of phase-change memory. These designs are simulated by using COMSOL 4.4 version software. The first step is design the conventional structure of phase-change memory to verify the theory that the multilevel storage cannot be achieved when heating directly to the memory layer which is the chalcogenide glasses.

The specific material properties have been set up for the design as stated in Table 1 to perform the ideal phase-change memory properties. There are two materials that have been fixed for both design which is the electrode (Copper) and substrate (Quartz). Other than that, the thickness of the memory layer has been varied to 50nm, 100nm, 150nm and 200nm to find the ideal thickness for the device structure according to the simulation of the temperature and the resistance.

Then, the most ideal result from the selected thickness will be tested with the different structure's width (500nm, 1000nm and 1500nm) for further analysis if there will be the possibilities to achieve a better simulation.

A. The Conventional Phase-Change Memory

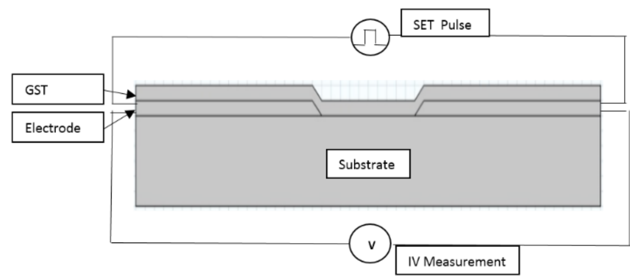


Figure 2: The Conventional Phase-Change Memory Design

Figure 2 above shows the conventional design of phase-change memory. For this design structure, the radical changes of resistance occurred with a single pulse applied with a certain voltage. It is because there is no insulator layer between the GST and the heater layer that cause difficulties to control the crystallization process of the memory layer, the applied pulse will directly to the GST without any heater layer.

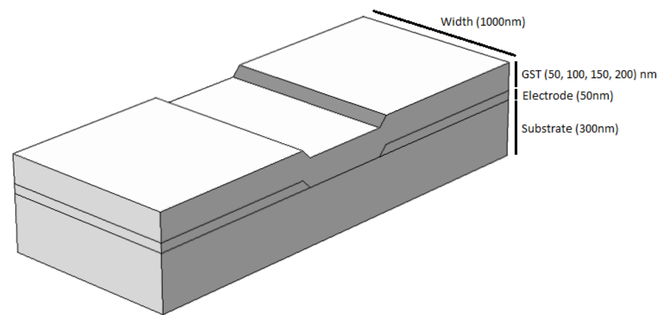


Figure 3: 3D Illustration of Conventional Phase-Change Memory

From the figure 3, the actual design structure can be seen clearly on how the phase-change memory looks like. The design is illustrated by finite element method using COMSOL 4.4 software. There is no heater layer on this structure in order to analyze the resistance drop to be compared with the proposed design.

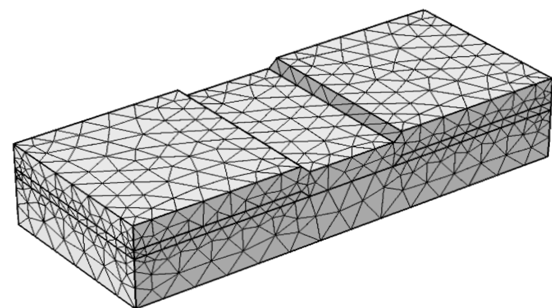


Figure 4: The Mesh of the Conventional Phase-Change Memory

Figure 4 shows the mesh of the structure. This step must be done before compute the design in order to set the size of the particle of the phase-change memory device.

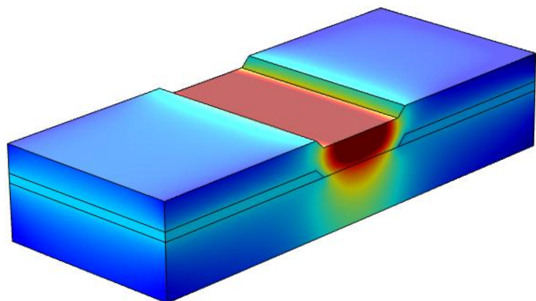


Figure 5: The Heat Distribution of the Conventional Phase-Change Memory

From the figure 5, it shows the heat distribution of the phase-change memory after been simulated. The red color on the middle structure represent the most hot spot while the blue one represent the colder spot of the structure. The electron will move on from the electrode to the other side when the memory layer completely in the crystalline phases.

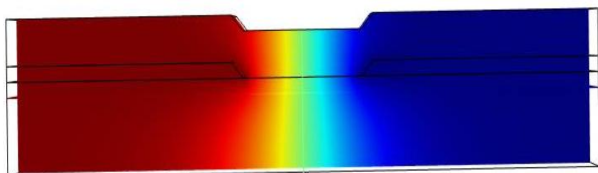


Figure 6: The Electricity of the Conventional Phase-Change Memory

Figure 6 above shows the potential current in the phase-change memory structure. The red one shows the highest potential current than the blue one. The result can be concluded that the electron is moved from the electrode to the other side since the GST is completely in crystalline state due to certain applied pulse and temperature.

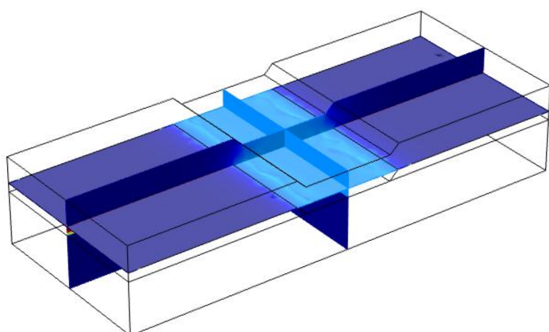


Figure 7: The Current Density of the Conventional Phase-Change Memory

The current density of the structure is shown in figure 7. The reason is to calculate the resistance drop in the memory layer by using the equation below.

$$\text{Rpcm} = \frac{\text{V}}{\text{JA}} \ldots\ldots\ldots\ldots\ldots (1)$$

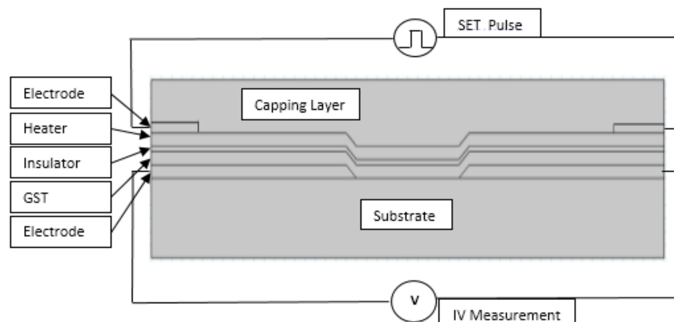
Where

Rpcm is the resistance on the phase-change memory (kΩ)

V is the applied voltage (V)

J is the current density (A/m^2)

A is the cross-sectional area (m^2)



B. The Proposed Phase-Change Memory

Figure 8: The Proposed Phase-Change Memory Design

Figure 8 shows the proposed phase-change memory design. The insulator is added between the memory and heater layer to ensure that the temperature in memory layer can be controlled well in term of the resistance to perform the multilevel storage device. Other than that, the insulator also used to prevent the electrical contact between the heater and memory layer. The capping layer, ZnS-SiO_2 is added to prevent the thermal heat loss from the separate heater layer to the outside of the phase-change memory. The materials for the separate heater and memory layer are $TiSi_3$ and GST, respectively. Between both layers, an insulator layer SiO_2 is inserted so that the layers will not electrically connected to each other.

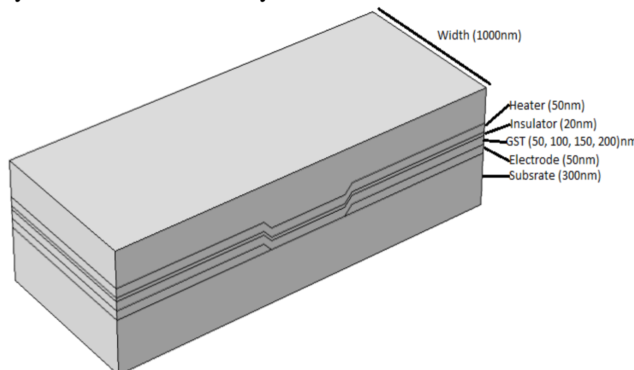


Figure 9: 3D Illustration of Proposed Phase-Change Memory

Figure 9 above shows the 3-dimensional design structure of the proposed phase-change memory device. From bottom, substrate > electrode > memory layer > insulator > heater layer > capping layer. The insulator is added between the memory and heater layer on this structure in order to analyze the resistance drop whether can perform the multilevel storage or not.

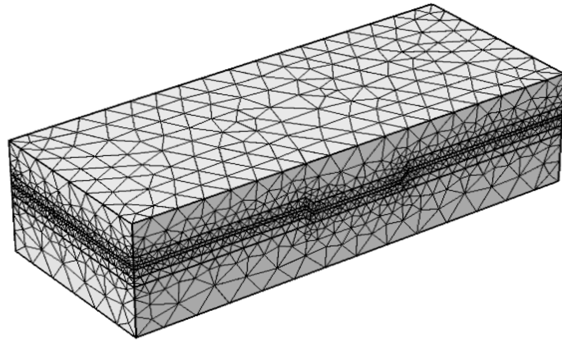


Figure 10: The Mesh of the Proposed Phase-Change Memory

Figure 10 shows the mesh structure of the proposed design. Same likes the conventional design, this step must be done before the simulation in order to set the size of the particle of the phase-change memory device.

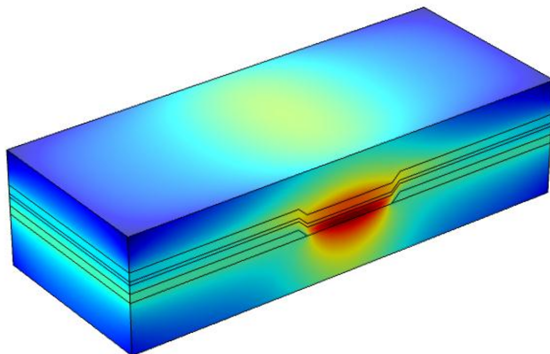


Figure 11: The Heat Distribution of the Proposed Phase-Change Memory

From figure 11, it shows the heat distribution of the phase-change memory after been simulated. The red color on the middle structure represent the most hot spot while the blue one represent the colder spot of the structure. The electron will move on from the electrode to the other side when the phase-change layer completely in the crystalline phases. The heat transfer is more stable due to the existence of the capping layer and the heat inside the structure will be trapped and not loss to the surrounding easily. It will lead to the efficient heating to the memory layer to change the phases from amorphous to the crystalline.

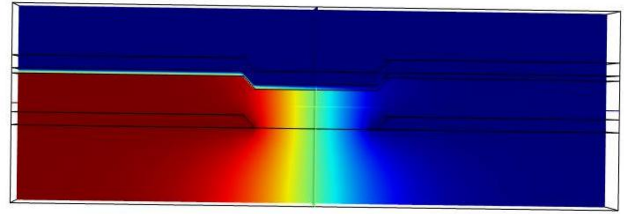


Figure 12: The Electricity of the Proposed Phase-Change Memory

Figure 12 shows the potential current in the phase-change memory structure. The red one shows the highest potential current than the blue one. The top layer of the structure shows that no current can pass through since there is an insulator that prevent the electrical properties to be emitted to the top layer of the structure. The simulation can be concluded that the electron is moved from the electrode to the other side since the memory layer is completely in crystalline phases due to the pulse applied.

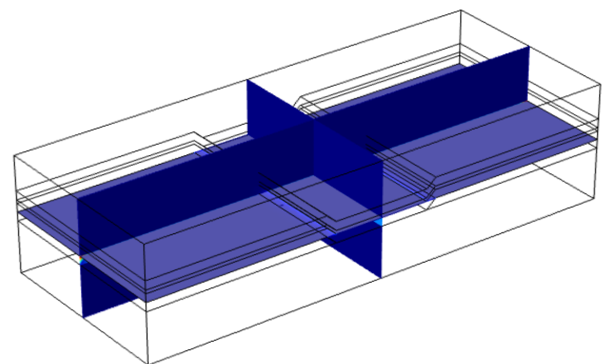


Figure 13: The Current Density of the Proposed Phase-Change Memory

The current density of the structure is shown in figure 13. The reason is to compute the resistance drop in the memory layer by using the equation same as the conventional design.

III. RESULT AND DISCUSSION

In this section, the deep discussion about result obtained from both design which is conventional and proposed will be interpreted and making the comparison between the two design results. The result that have been computed and observed have been recorded. The result will be compared in term of structure design size, device speed, the abality to perform multilevel storage.

PART A: THICKNESS OF MEMORY LAYER

This section will focus on the thickness of the memory layer which is the GST. The thickness will be varied to 50nm, 100nm, 150nm and 200nm for the both conventional and proposed design to compute the temperature and the resistance of the phase-change memory.

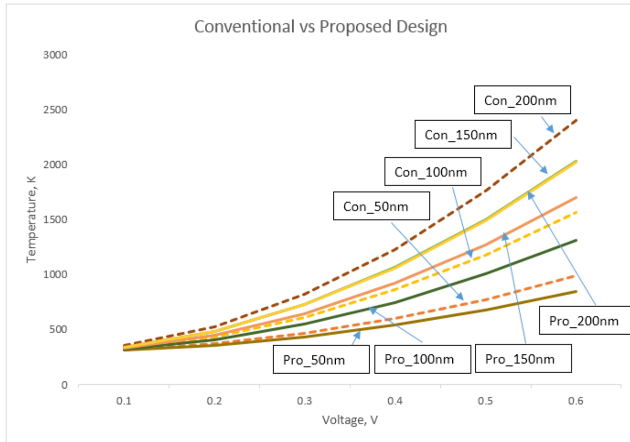


Figure 14: The Comparison of Temperature of Both Phase-Change Memory Design

From the figure 14, it shows the simulation of the temperature for both conventional and proposed design of phase-change memory. The highest temperature is from the conventional design with 200nm of GST's thickness while the lowest temperature achieved is from the proposed design with 50nm thickness of GST. The best and the worst result can be defined by the graph which is the phase-change memory need to be in range 450K to 900K in order to be in crystalline phases.

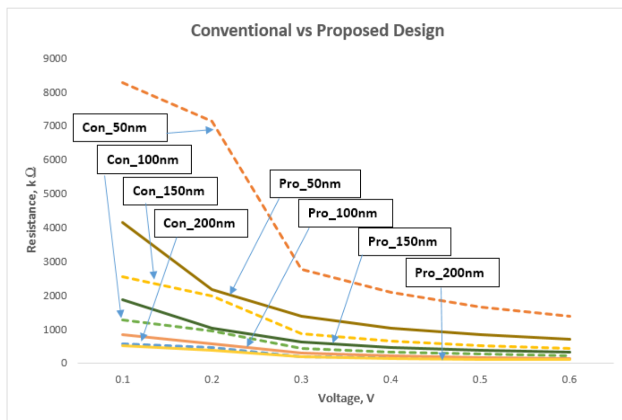


Figure 15: The Comparison of Resistance of Both Phase-Change Memory Design

Figure 15 shows the simulation of the resistance for the both conventional and proposed design of phase-change memory. The highest resistance is from the conventional design of 50nm thickness while the lowest is conventional design with 100nm thickness. But in this case, the temperature of phase-change memory will be a priority since the device will function in certain range of temperature. Also the resistance need to decrease gradually instead of radical decrement to perform the multilevel storage. Furthermore, the lowest the resistance the faster the device.

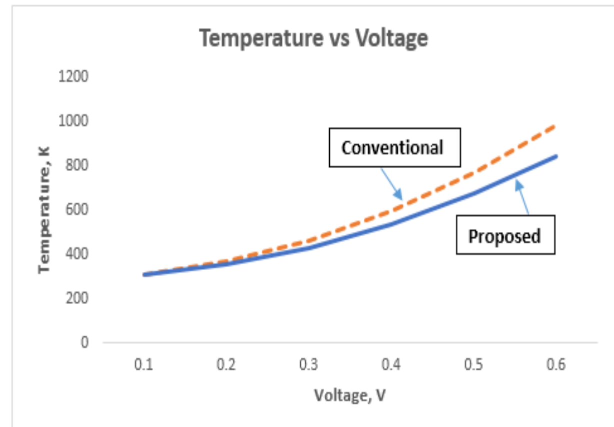


Figure 16: The Comparison of the Best Simulation

From figure 16, it shows the comparison in temperature between the 50nm thickness of conventional design and the 50nm thickness of proposed design which is the best in temperature from other results. As can see, the proposed design perform much better since the temperature is below 900K at 0.6V which is the GST is in the crystalline phases while the conventional design is out the range at the 0.6V in term of the temperature.

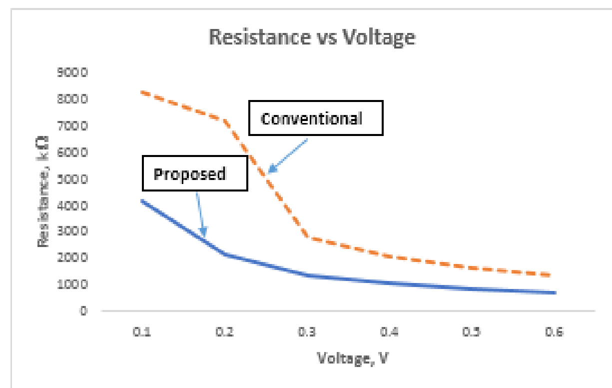


Figure 17: The Comparison of the Best Simulation

From figure 17, it shows the comparison in resistance between the 50nm thickness of conventional design and the 50nm thickness of proposed design which is the ideal resistance from other results. The graph shows the proposed design perform much better since the resistance is decreasing gradually while the conventional design is decreasing radically which is cannot perform the best multilevel storage for the phase-change memory.

PART B: THE STRUCTURE'S WIDTH

The best result achieved on Part A will be analysed much deeper in this part. The 50nm thickness of GST for both design will be simulated by vary the structure's width to 500nm, 1000nm and 1500nm. The data for the simulation as shown below:

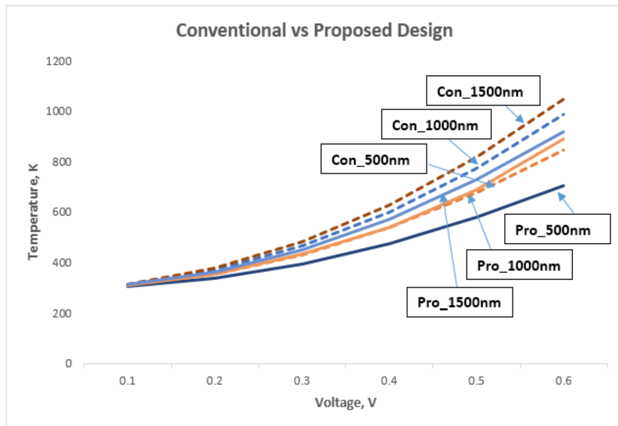


Figure 18: The Comparison of Temperature of Both Phase-Change Memory Design

From the figure 18, it shows the simulation of the temperature for both conventional and proposed design of phase-change memory. The highest temperature is from the conventional design with 1500nm of structure's width while the lowest temperature achieved is from the proposed design with 500nm width of structure. The best and the worst result can be defined by the graph which is the phase-change memory need to be in range 450K to 900K in order to be in crystalline phases.

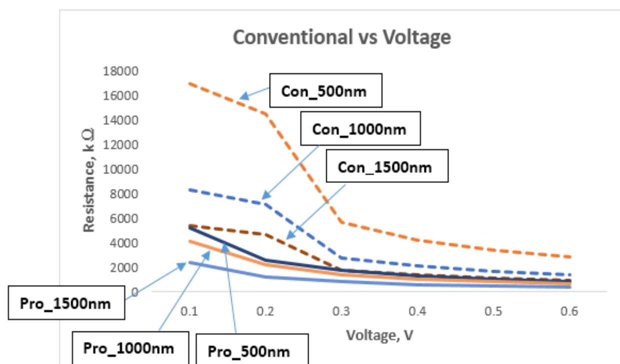


Figure 19: The Comparison of Resistance of Both Phase-Change Memory Design

Figure 19 shows the simulation of the resistance for the both conventional and proposed design of phase-change memory. The highest resistance is from the conventional design of 500nm width while the lowest is proposed design with 1500nm width. But the temperature of phase-change memory will be a priority since the device will turn on in certain range of temperature only which is from 450K to 900K. The resistance also need to decrease gradually instead of decrease radically in order to perform the multilevel storage.

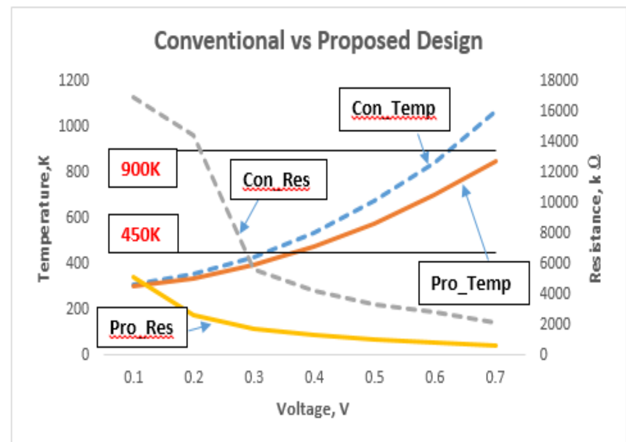


Figure 20: The Overall Comparison between Conventional and Proposed Design of the Best Parameters and Results

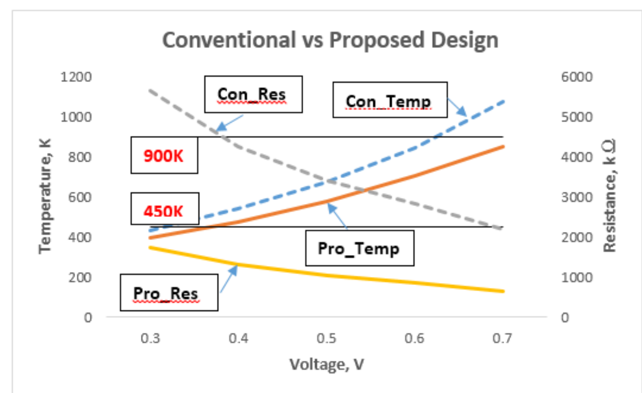


Figure 21: The Overall Comparison between Conventional and Proposed Design of the Best Parameters and Results (Zoom in Graph)

From figure 21, it shows the combination result between the best result of conventional and proposed design of phase-change memory. After a deep analysis about the effect of parameters to the multilevel storage ability, the best parameter will be 50nm thickness and the 500nm width for proposed design as shown in figure 20 and 21. The proposed design perform much data storage than conventional design within range 450K to 900K.

A. *Size of the structure*

To design something that can fulfill the current consumer needs especially the electronics product is to gain a smallest device as can be. From this design, both conventional and proposed design had been simulated with a small scale in term of width, length and the thickness (in nano meter).

But there also will be the disadvantages to the design which is from the material properties limits. For a certain scale of parameters, the design would not function correctly due to the saturation region caused by the applied pulse and the device will burn and broke down. So the device's size should be controlled for a certain measurement to prevent the malfunction of the outcome product.

B. *Device speed*

Theoretically, the phase-change memory device will perform faster with a smaller resistance. According to the result achieved, it shown that the proposed design is more efficient in term of speed than the conventional design due to the lower resistance.

The electron can move faster from one electrode to the other side since there is low internal resistance of the proposed design as shown in figure 21. This can ensure that the data written and read can be performed much better and faster than conventional design of the phase-change memory.

C. *The ability of multilevel storage*

The first condition to change the amorphous to the crystalline phases is the temperature must in range 450K to 900K. According to the figure 21, the proposed design seemed had more points in that range compared to the conventional design that can assure more data can be stored in device. Furthermore, the resistance drop for proposed design is more gradual and stable than the conventional design which is had a radical decrement of the resistance for a certain SET pulse applied.

IV. CONCLUSION

This work shows the simulation of temperature and the resistance changes of the GST for both conventional and proposed design with separate heater layer and some different parameters as modelled using COMSOL 4.4 Multiphysics. As the results, it can be clarified as following:

- Regarding to the thickness of the memory layer, it shows that the 50nm of proposed design gave a better simulation compared to the 50nm conventional design in term of multilevel storage.
- The proposed design got a better range in temperature which is from 450K to 900K in order to change the phases of GST from amorphous to crystalline.
- The proposed design with heater layer gave a better resistance decrement than the conventional design.
- As shown in Part B result, the 500nm width gave a better simulation after be analyzed using the 50nm thickness of GST.
- The most ideal parameters for the multilevel storage phase-change memory are 50nm thickness of GST and 500nm width for the proposed design as shown in figure 21.
- It shows that the separate heater layer can ensure the multilevel storage instead using the structure with direct heating to the memory layer.

V. ACKNOWLEDGEMENT

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VI. RECOMMENDATION

For better future recommendation, there's a suggestion to improve the phase-change memory configuration by combining the better features from other configuration. For example, the GST was used as the memory layer which can perform a certain multilevel storage limit. Alternatively, the different phase-change material can be used which is more suitable and compatible to perform the bigger capacity of data storage. This may improve many features such as the data written and read speed, the minimum voltage applied, the sizes of the device, the resistance changes of the memory layer and the temperature's range to change from amorphous to the crystalline phases. The suggested design also should reduce the total power consumption. Other than that, the design also must able to increase the cycle of the phase-change memory since the GST only can up to 10^6 cycles. Furthermore the reducing of area and the sizing of phase-change memory also need to be considered for a better space especially for the smaller device of nonvolatile memory devices. The perfect phase-change memory

cannot be achieved since there are many possibilities may occur in one design. So that, the further study and hardworking is needed to ensure that the better design can be created for a better life in technologies especially for the nonvolatile memory devices.

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