Integrated Circuit Design of Readout Interfacing Circuit for MEMS Resonator Characterization

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***Abstract*- The paper present the implementation of readout interfacing circuit (ROIC) for MEMS Resonator characterization of natural frequency. The MEMS Resonator will produces a vibration of current at unknown frequency and at the difference condition. The purpose of the readout interfacing circuit is to convert the current from MEMS Resonator output and amplify the signal. The readout interfacing circuit is divided into 4 parts (i) design of the basic operational amplifier that is used as a subcircuit (ii) design of transimpedance amplifier (iii) design of the instrumentation amplifier and (iv) design the readout interfacing circuit. Circuit architecture and layout of the design are presented. The readout interfacing circuit was designed using 0.13um Silterra technology file with 2V power supply. Two type of operational amplifier are proposed using a different specification and model. The simulation result shows that the operational amplifier achieve the specification such as 55.75dB of open loop gain, 58.00dB of CMRR and 8.32mV offset voltage. In addition, the functionality of the read out interfacing circuit has been verified and be able to detect the natural frequency of the MEMS resonator.**

Keywords — MEMS Resonator, Open Loop Gain, CMRR, Offset Voltage

I. INTRODUCTION

MEMS is defined as Micro Electro Mechanical System. The integration of MEMS devices with microelectronic circuits is a promise of miniaturization and modular System On Chip design for the next few years [7]. MEMS Resonator provides a promising alternative for quartz crystal as accurate timing devices in oscillator circuits for modern data and communication application. Based on that, this project was conducted to design the integrated circuit design to represent the electrical part of the device. The MEMS Resonator is relatively large because it consists of mechanical and electrical in its architecture but it is possible to implement the electronic design into microelectronics which is significantly smaller and could be built in the single package. In considering the previous references, the main contribution of this work is to design the integrated circuit that can be implemented in the device and also be able to miniaturize the size of the device. Besides that, conventionally the readout circuit implementation on PCB consisting of separate IC will introduce noise to the MEMS signal. Therefore the integrated circuit of readout interfacing for MEMS resonator characterization was designed. The main purpose of designing the readout interfacing circuit at the integrated circuit level can reduce a lot of interference as this allows the sensor, that is silicon based and the circuit to be monolithic. The works are divided into 3 parts which are schematic design, simulation and testing and layout design.

Figure 1 depicted the overall overview of the readout interfacing circuit. The transimpedance amplifier is used to convert the current vibrations from the output of the MEM resonator sensor into voltage. The output voltage is fed into an instrumentation amplifier to compare the MEMS resonant frequency and a controlled sweep frequency to detect the unknown natural frequency of the device. The controller swept frequency come from the signal generator is swept from minimum to maximum values and the output waveform of the instrumentation amplifier is observed by using an oscilloscope. The instrumentation amplifier will detect the matching frequency and display a sinusoidal waveform. If the frequency is matched, it will display a sinusoidal waveform without any distortion otherwise it will display a distorted waveform.

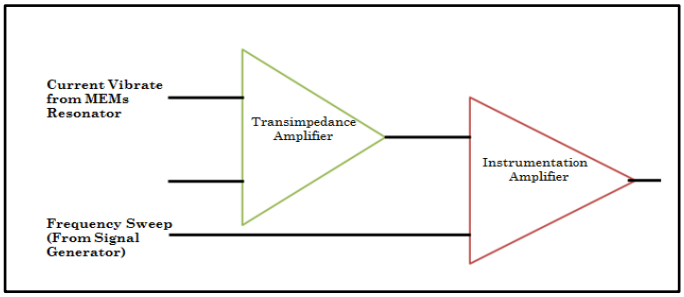

Figure 1: Overview of Read Out Interface Circuit

II. METHODOLOGY

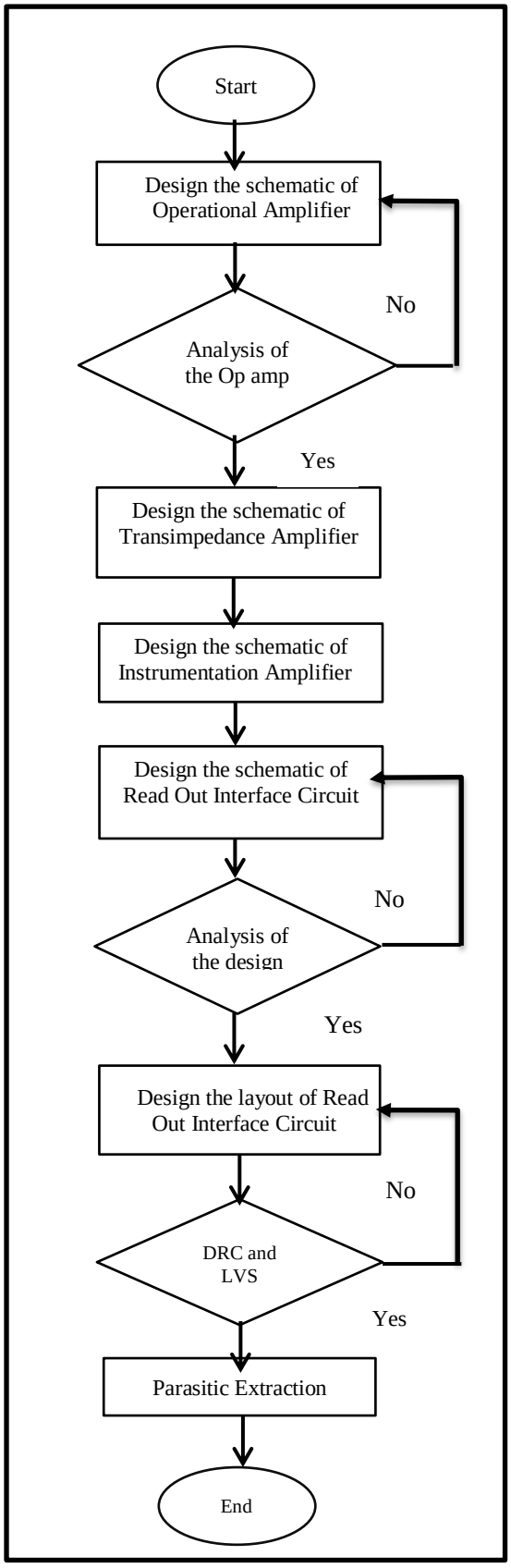

Figure 2: The design Flow Chart

The integrated circuit of readout interfacing for MEMS Resonator was designed using custom integrated circuit design approach as depicted in Figure 2. The schematic of operational amplifier were designed using Silterra 0.13µm technology files with a specific design requirement. The characteristic of the operational amplifier such as the gain, offset voltage, common mode rejection ration (CMRR) and the output swing was analyzed using simulation software. Then, the operational amplifier is used as a module that instantiated to form a transimpedance and an instrumentation amplifier. Afterward the project proceeded with designing the schematic of the overall read out interface circuit. Further proven of the design was performed to ensure that the design met the requirement and be able to detect the natural frequency of the MEMS Resonator. Next, the layout of the read out interface circuit was carried on based on the using Silterra design rule and the LVS (layout versus schematic) was checked to make sure that the layout is equivalent to the schematic connection. The parasitic extraction was performed to calculate the parasitic element of the design which may be degraded the performance of the design.

III. **RESULT AND DISCUSSION**

The main functionality of the readout circuit is an amplification of MEMS resonator output current that is expected to be produce as resonance of the MEMS in a specific shape in the hundreds of MHz range and to be very weak [7]. The presence of the read out strategy was reported in this section including the schematic, characteristic and layout of the design.

A. Two Stage Operational Amplifier

A set of requirement for the operational amplifier is listed in Table I.

TABLE I. DESIGN SPECIFICATION OF TWO STAGE OPERATIONAL AMPLIFIER.

Specification	*Value*
Supply Voltage	±1.5V
Input Common Mode Range (ICMR)	-0.2V to 1V
Output Range	± 1V
Slew Rate	±10V/µs
Gain Bandwidth	10MHz

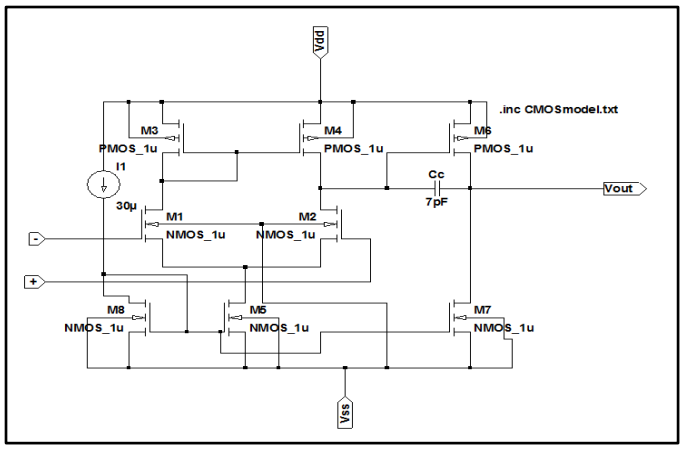

Figure 3: Design Architecture of Two Stage Operational Amplifier

The two stage amplifier consists of cascade voltage to current and current to voltage stage. The first stage consists of a differential amplifier that converting the differential input voltage to differential currents. Then the output of the differential amplifier is applied to the current mirror load to recovering the differential voltage. The second stage consists of common mode MOSFET will convert the second input voltage into current and finally the current sink load will convert the current to voltage at the output stage.

The ratio for each transistor are calculated based on the appropriate method and the summary of the ratio are shown in the Table II below.

TABLE II. ASPECT RATIO OF TRANSISTOR

Transistor	*Ratio (W/L)*
M1	2.4
M2	2.4
M3	44
M4	44
M5	3.2
M6	44
M7	29

Once designed the operational amplifier schematic, the analysis of the design is the next step. The design characterization was divided into two parts which is DC and AC characterization. The DC characterization allowed verification of the DC performance as a function of the input DC voltage. On the other hand, the AC characterization is the verification of the AC performance along with time and frequency.

The output waveform obtained in Figure 4 is the open loop gain of the two stage amplifier with 10pF load capacitance. The open loop gain is defined as the ratio between input and output voltage. From the result, it's shown that the open loop gain of the design is 54.34dB.

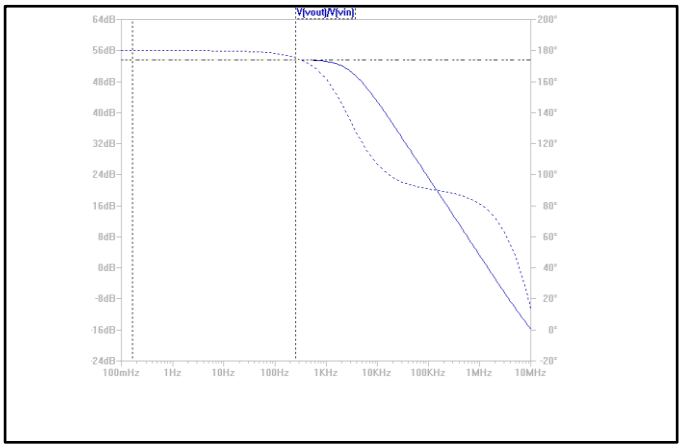

Figure 4: Output Waveform of Open Loop Gain

The Common Mode Rejection Ratio (CMRR) is defined as the ratio between differential gain and common mode gain. Figure 5 shown the output waveform of CMRR of the two stage operational amplifier which is 55.34dB.

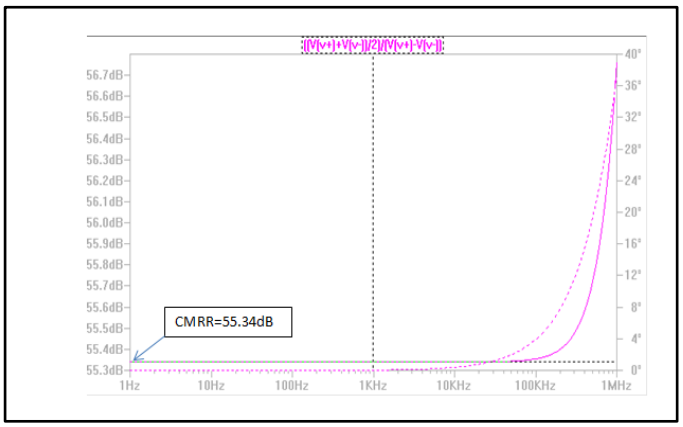

Figure 5: Output Waveform of Common Mode Rejection Ratio

B. Low Voltage Operational Amplifier

There are two types of Op-amp design either single supply design or rail to rail supply design. The difference between the operational amplifier in Figure 6 below with the previous Op-Amp is it used a single rail supply. Table 3 shown the list of requirements of the design.

TABLE III. DESIGN SPECIFICATION OF LOW VOLTAGE OPERATIONAL AMPLIFIER

Specification	*Value*
Supply Voltage	2V
Input Common Mode Range (ICMR)	1V to 2.5V
Output Range	0.5V to 1.75V
Slew Rate	±10V/µs
Gain Bandwidth	10MHz

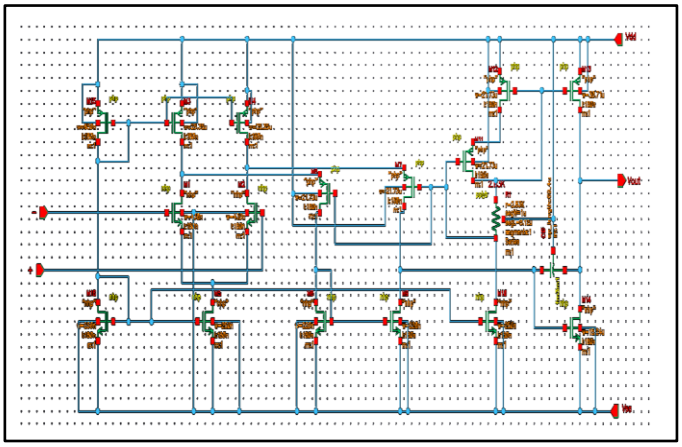

Figure 6: Design Architecture of Low Voltage Operational Amplifier

The low voltage operational amplifier in Figure 6, consist of 3 stages which are input stage, gain stage and output stage. The input stage is the n-channel differential amplifier which gives the widest possible input common-mode range. The p-channel source are connected to the output of the differential amplifier to give the maximum input common mode voltage and allow the power supply to vary without limiting the positive input common-mode voltage [10]. Current from differential output are folded through transistor M6 and M7 and converted to single ended signals with n-channel current mirror. The simple class A output stage using Miller compensation is used for the second-stage gain [10].

TABLE IV. ASPECT RATIO OF TRANSISTOR

Transistor	*Ratio (W/L)*
M1	6.38
M2	6.38
M3	12.23
M4	12.23
M5	10.34
M6	24.47
M7	24.47
M8	1
M9	1
M10	10.34
M11	24.47
M12	24.47
M13	30.76
M14	253.94
M15	25.16
M16	10.34

Table IV summarizes the aspect ratio of transistor for low voltage operational amplifier. The transistor sizing is determine determined based on hand calculation and process parameter that define by the technology.

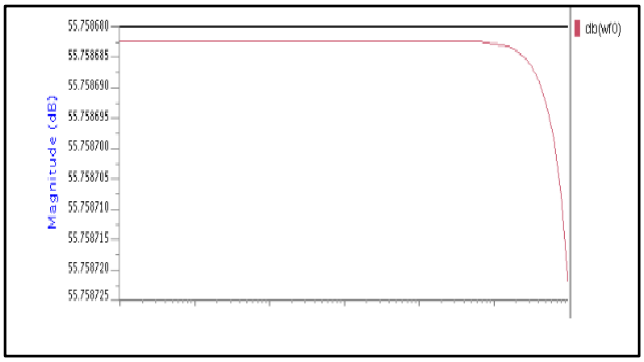

Figure 7: Output Waveform of Open Loop Gain

Figure 7 shown the open loop gain of the low voltage op-amp with 10pF load capacitance. From the result, it's shown that the open loop gain of the design is 55.75dB.Besides open loop gain and CMRR, the offset voltage also an important characteristic that needs to be analysed when design an operational amplifier. The offset voltage is determined by applying a zero voltage at the input terminal. Ideally, the output should be zero when the input is grounded but in reality there are slightly different voltage at the input terminal [10-11]. The output that produce when the input is zero is known as offset voltage. Output waveform below shown the offset voltage of the design which is approximately 8.32mV.

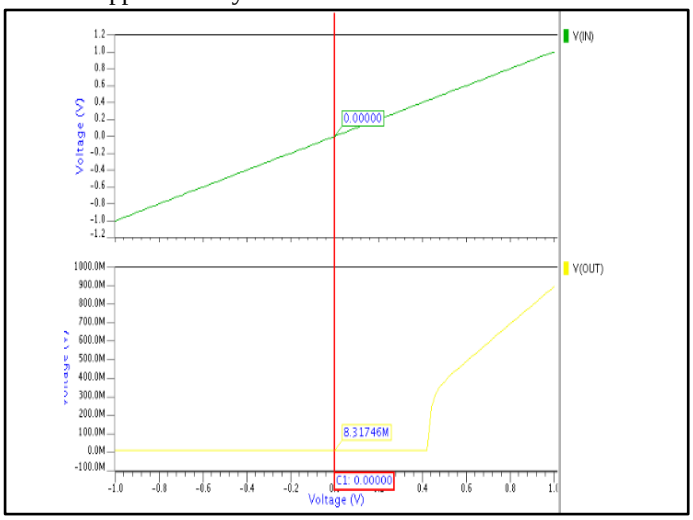

Figure 8: Output Waveform of Offset Voltage

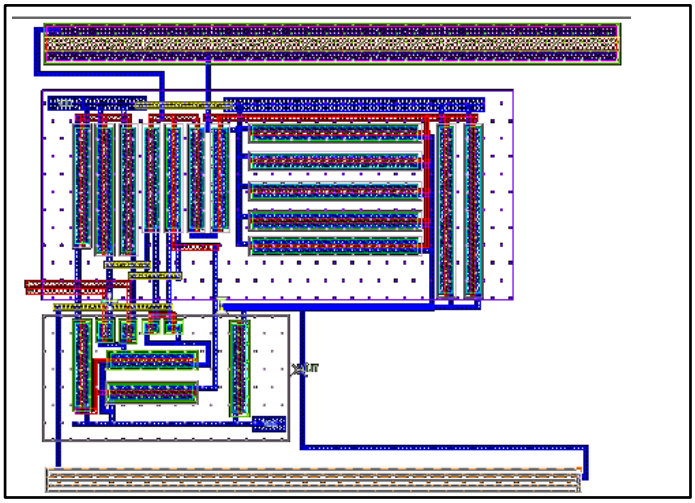

Figure 9: Layout View of Low Voltage Op amp

The layout of low voltage op-amp circuit shown in Figure 9 is done using Mentor Graphic software .The layout passes both DRC and LVS .

TABLE V. CHARACTERISTIC OF OPERATIONAL AMPLIFIER

Performance parameter	*Two Stage Op amp*	*Low Voltage Op amp*
Power Supply Current	30uA	20uA
Open Loop Gain	53.34dB	55.76
Offset Input Voltage	9.36mV	8.32mV
CMRR	55.34bB	58.00 dB

C. Transimpedance Amplifier

The transimpedance amplifier is designed to convert the vibrate current from MEMS Resonator into voltage so that it can be used in the instrumentation amplifier. Figure 10 below show the design architecture of transimpedance amplifier. The op amp is used as a sub circuit in transimpedance amplifier. The current source is used in the design to represent the output of the MEMS resonator.

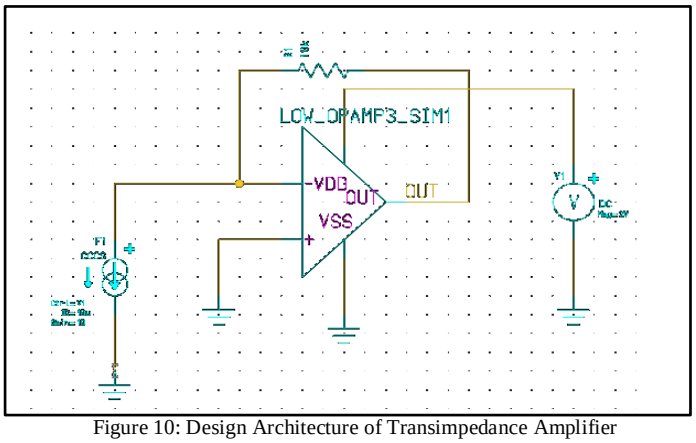

Figure 10: Design Architecture of Transimpedance Amplifier

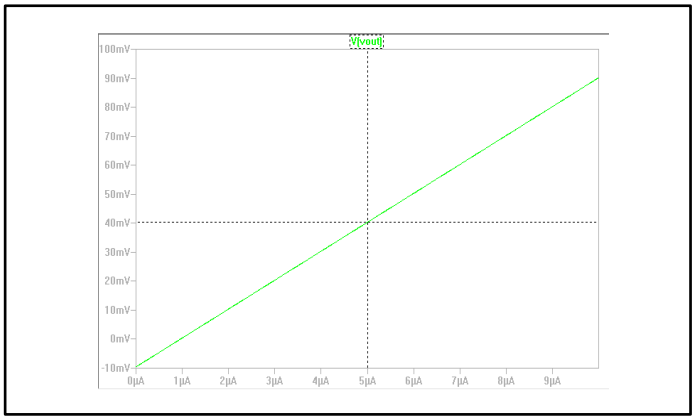

Figure 11: Output Waveform of Transimpedance Amplifier

The simulation result showed the change of voltage when the current source is swept from 0 to 10uA. Below show the hand calculation of the output voltage compares with the simulation result. Its proving that the transimpedance amplifier is successfully design to convert current into voltage.

When I=5µA, R=10k

V =IR +offset voltage)… (Eq.1)

=(10µ)(10k)-8.32mV

=(50mV)-8.32mV

=41. 68mV

D. Instrumentation Amplifier

Instrumentation amplifier is used in applications where a small differential output voltage from a sensor must be accurately amplified in the presence of strong common-mode input voltage [3]. This conventional three op-amp instrumentation amplifier in Figure12 is widely used because it provides a high common-mode rejection and high input impedance [3].

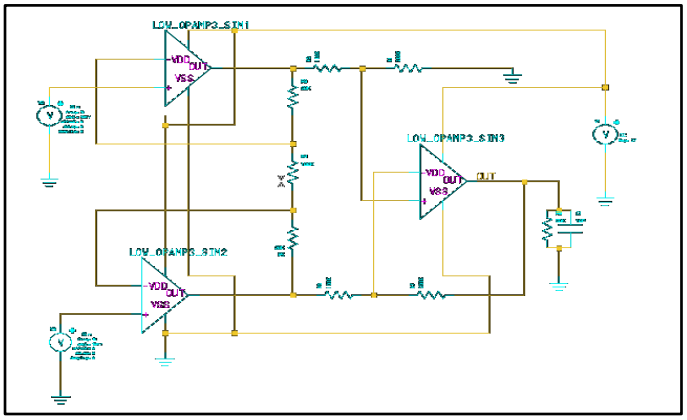

Figure 12: Design Architecture of Instrumentation Amplifier

The simulation result shows that the instrumentation amplifier has a DC gain of about 65.07dB as shown in Figure 13. The offset voltage of the design is approximately 34.69mV.It was designed to drive a capacitive load of 10pF. From the result, its show that the offset voltage for instrumentation amplifier is large compared to the single operational amplifier. The instrumentation amplifier has a large offset voltage because the offset voltage is equal to the sum of individual offset voltage for each op-amp.

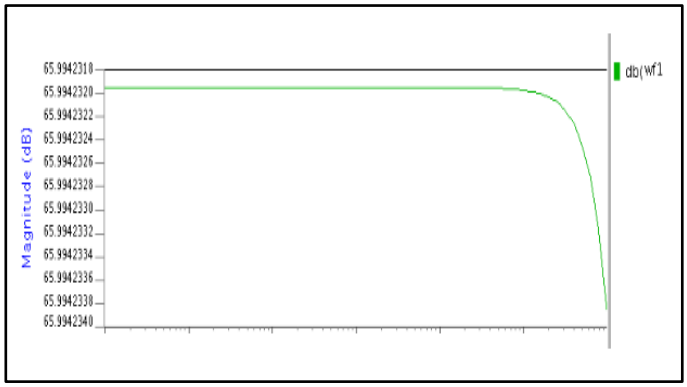

Figure 13: Output Waveform of Open Loop Gain

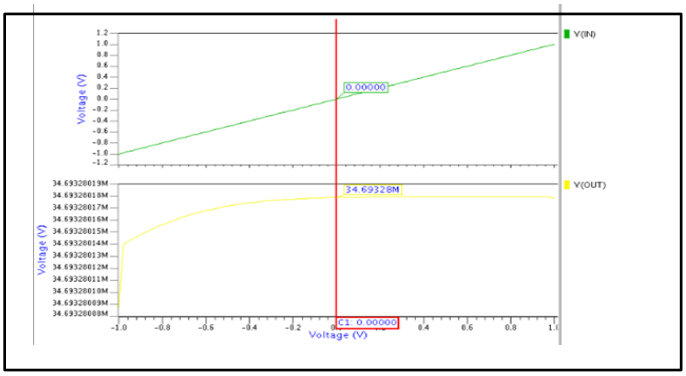

Figure 14: Output Waveform of Offset Voltage

E. Readout Interfacing Circuit

The configuration proposed othe readout interfacing circuitit is based on transimpedancece anthe instrumentation amplifierer as shown in Figure 15. For the simulation purpose the current source is connected to the input of the transimpedance amplifier to represent the current flowing out the MEMS Resonator when electrostatically excited. Output voltage from transimpedance is amplified through instrumentation amplifier. Then, the instrumentation amplifier will differentiate the signal between both input terminal.

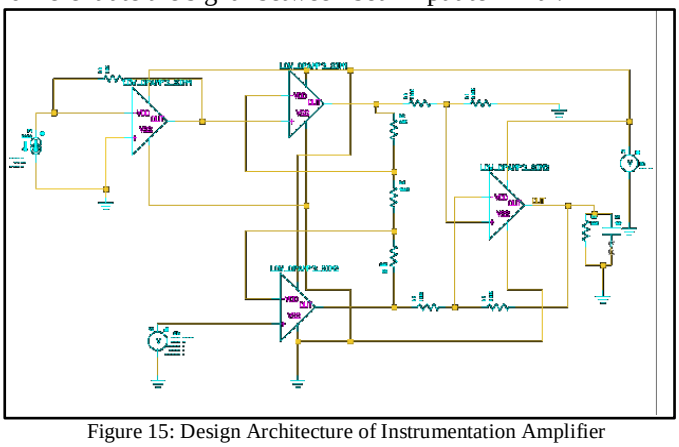

Figure 15: Design Architecture of Instrumentation Amplifier

The output waveform that obtained in Figure 16 is the output of the readout interfacing circuit when both input terminal has a match signal. During this simulation, one of the instrumentation amplifier input is connected with 10mV voltage with 1kHz frequency. The input current of 10µA with 10kΩ resistor is connected to the transimpedance amplifier to produce an approximately 10mV output voltage that is connected to the other input of the instrumentation amplifier. Since the signal is matched, so that the sinusoidal output that produce has an equal amplitude and frequency.

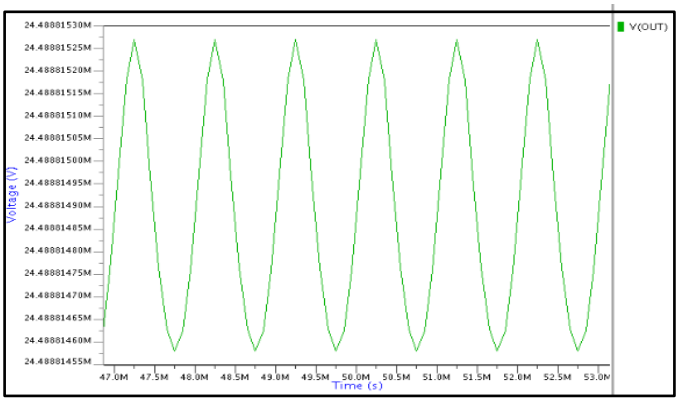

Figure 16: Output Waveform of Read Out Interface Circuit

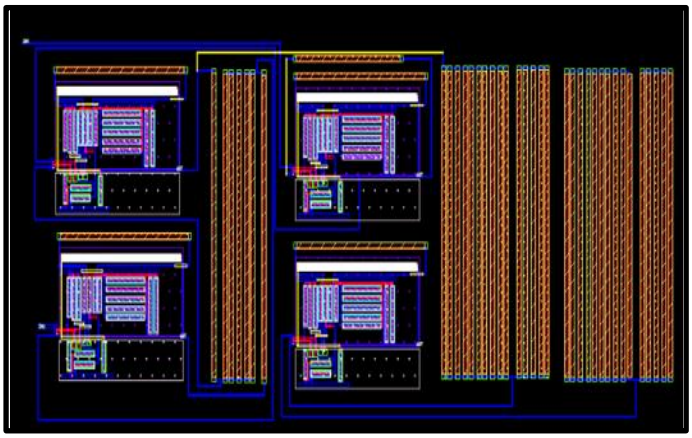

Figure 17: Layout of Readout Interfacing Circuit (ROIC)

IV. CONCLUSION AND FUTURE WORK

In this paper, it demonstrated the readout strategy for MEMS Resonators based on transimpedance and instrumentation amplifiers. The readout integrated circuit has been designed using 0.13um technology and the character of the design has been performed using a simulation software. Simulation results showed that the integrated circuit of MEMS Resonator will allow extraction of electrical parameter in MEMS Resonator as well as be able to miniaturize the size of the devices.

As a recommendation, tapeout the design in order to verify the functionality of the design at the hardware. Besides that, the design can be interface with MEMS Resonator to investigate the functionality of the design when its apply to an actual application.

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Figure 12: Design Architecture of Instrumentation Amplifier

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