Nanoelectronics Implementation Of Logic AND/OR With Memristors

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Abstract— A memristor is a two terminal passive component which is a non-linear circuit element relating to charge, q and magnetic flux linkage, ϕ [5]. This research focuses on implementing the component into hybrid electronic device that would give identical result to its identical device which is fully CMOS structured. The research include integrating spice-model of the memristor into appropriate software for simulation, analysis on particular aspects which is the speed and power dissipation and then comparing the hybrid of the CMOS and memristor to a more familiar full CMOS device. The logic AND and OR device aspects of the hybrid is similar, only the full adder output sum did not match. According to the analysis, the hybrid design would give better power dissipation and smaller layout size compared to the fully integrated CMOS design only its disadvantage is at its speed but would be solved by implementing buffer to the output, without overcompensating the size of the design.

Keywords— **Memristor, Hybrid CMOS-memristor, Logic AND, Logic OR, full adder.**

I. INTRODUCTION

The breakthrough of a new passive device element was discovered in 2008 by the HP Labs team. The transistors has been used as the basic building block in electronic devices since the creation of the transistor which comes to its prime in1956[1]. The transistor was much bigger than nowadays hence the shrinking of the transistors was inevitable in order to construct much better devices which starts subsequently as soon as the researchers realize the potential of it. Intel co-founder Gordon E. Moore has said that in years to come the number of components in and integrated circuit, will double every year [2][3], whereby it has so far been proven true. But the shrinking process which has been going for about 50 years since the creation of transistors is nearing its end which could be approximated by the time it shrinks to an atomic size which would be impossible [4]. This limitation might be prolonged with the realization of the fourth passive element, the memristor. The memristance behavior in thin films are basically how memristor came to fruition and will be discussed is the hysteretic behavior given out by electronic devices. This is how it all started [9-11], which would date back to nearly 50 years when discovered by Leon Chua. It is realized by HP labs research group headed by R. Stanley Williams during their research on crossbar array potential in electronic circuitry. Prior to their discovery the memristor was officially presented by a mathematician Leon Chua who discovered a fourth missing element that would connect the fundamental circuit variables: electric current I, voltage V, charge q and magnetic flux ϕ. Thin film technology is being applied whereby a thin semiconductor film of thickness D is wedged between two metal contacts. The thin film are made out of layer of TiO2 , which acts as an insulator and TiO2-x(titanium dioxide with oxygen vacancies), which acts as the conductor, the metal contacts are made out of platinum [4,5].

The device is bias with voltage supply for it to function. When external voltage v(t) is applied across the two terminal device, the charged dopant will start to drift which will move the boundaries between the two region . Positive bias will repel the oxygen vacancies TiO2-x thus making the boundary of the doped region bigger, low in resistance and hence turning the device 'on' and if negative bias is being applied whereby the device turns 'off' and resistance is high, depending on the position of the layer and also the external biasing..

II. RESEARCH OBJECTIVE

The proposed objectives for this project is to use a spice model of a memristor that is identical to the real memristor which is envisioned by L. Chua. This spice model memristor would consistently replicate identically its memristive behavior. By varying the values would give variable value of the memristance like time, resistance ratio and width. Besides that is to implement the memristor model created in spice toward designs. The design would specifically be realize in devices which usually consists of CMOS as its main attributes. Thus coming up with a CMOS-memristors hybrid. Other than that would be to come up with a layout design on the logical architecture of

normal digital device using CMOS technology and digital device with memristor implementation. The CMOS-memristor hybrid would be designed in estimation of its applied sizes. Finally to investigate the memristance implementation on device designed. Comparison of the two normal CMOS digital device design and the hybrid design in terms of outputs and the architecture would be considered. The performance would also be analyzed indistinctly in terms of speed, delay or size.

III. METHODOLOGY

In order to design a digital logic device that could incorporate the memristor component, a spice model of a memristive system would be used and integrated into spice software which in this case is the LTspice IV. The software would be used for simulation in order to get the appropriate results that would make it comparable to the original design of the CMOS digital device. The memrestive modeling that would be used is the spice modelings of MEM-Systems [6] were created by the Biolek brothers and Viera Biolkova of Czech Republic . This particular model corresponds greatly with the responses obtained by HP Labs. The spice-model would be integrated into LTspice where both the digital devices would be designed. The devices would have the same functionality but different designwise. The model would include the subcircuit of the memristor, with the settings of Ron at 1kΩ and Roff at 100kΩ with Rinitial at 80kΩ. The state equation modeling following Eqn.1 only that it adds a window function to make it non-linear. The resistive port modeling to give it resistive value and the window function so that the *w* would not reach D or 0 during the simulation which is not possible[14]

$$M(q) = \mathcal{R}_{OFF}\left(1 - \frac{\mu_V \mathcal{R}_{ON}}{D^2} q(t)\right)$$

Eqn. 1: memristance of the system since Ron<<Roff is actually based on this two equations, v=R(w)i and dw/dt = I from L. Chua's most basic mathematical definition of a current-controlled memristor for circuit analysis is the differential form [11]

A. Logic Design Choice

The logic design using the memristor could be done in three known ways at the moment. Hybrid[10], IMPLY logic[12] and MAGIC[13] (memristor aided logic). The hybrid is basically a combination of both memristor and CMOS device, IMPLY logic would be using the material implication in designing the logic, this where the crossbar array is put into context while MAGIC use only memristors to make logical devices. The Hybrid design was chose due
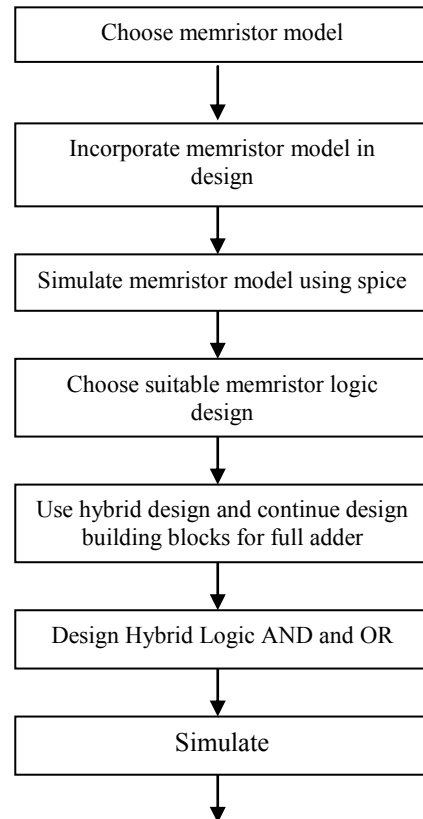
to its simplicity and similarity to the known full CMOS configuration of a full adder

B. Logic AND and OR

In any logic design logic AND and OR are important component in designing logic designs. Logic AND and OR the former could be designed by positively biasing the memristor with inputs and the later negatively biasing the memristor with the input.

C. Full Adder Design

Full adder arithmetic could be design in a few ways using memristor as mentioned before, the method that will be using here is hybrid memristor-cmos. After simulating the right result for memristive digital device which matches the CMOS design, the memristor crossbar array would be tested in terms of its performance from LTspice software in term of speed, power consumption and size. It will then be compared to the CMOS design at exact same terms. The whole methodology process could be summarized in the flowchart below.

Figure 3: Hybrid circuit configuration of a logic AND device with output of hybrid circuit configuration.

C. Logic OR

Figure 4: Hybrid circuit configuration of a logic OR device with output of hybrid circuit configuration.
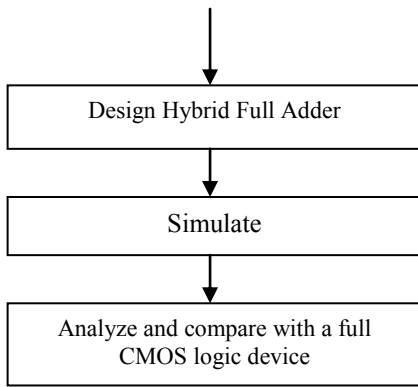

Figure 1: Flow chart for the whole methodology process

IV. LOGIC EXPERIMENTATION AND SIMULATIONS

The SPICE model of the memristor was incorporated into LTSPICE and biased as to show its hysteresis behavior. This could be seen in figure 2.
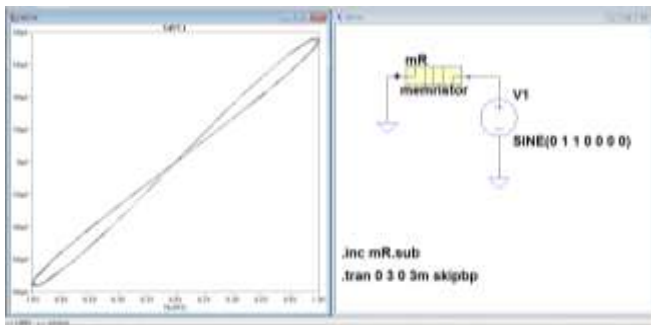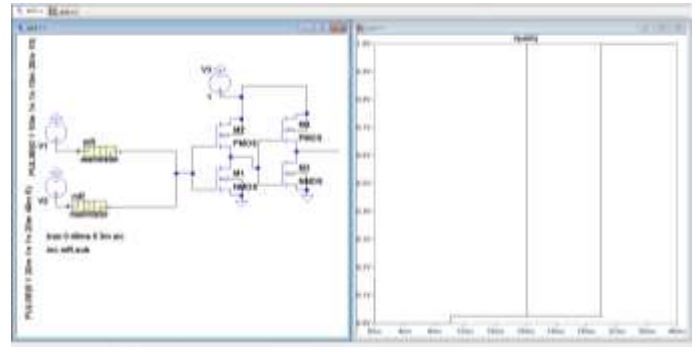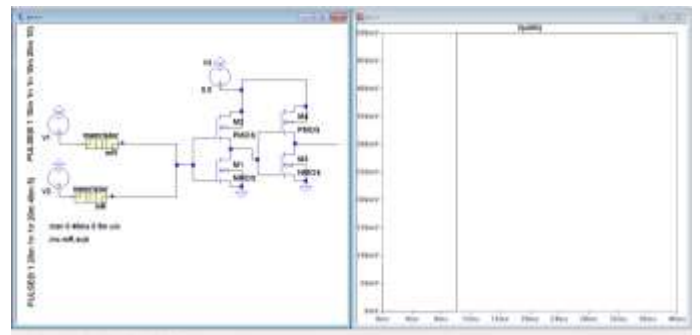
A. Putting Memristor Model into LTSPICE

Figure 2: memristor biased with sinewave with the output result of the single memristor

This is the expected output of the memristor device according to the spice-model depicted above. Since the model has been incorporated, the logic design of the devices that would make up a full adder was designed and tested. The design would be hybrid between memristor and CMOS logic whereby the CMOS logic that would be used are only inverters to replicate the function of an XOR logic gate. The memristor logic gate that will be applied is the AND and OR.

Figure 3 shows the configuration of an AND hybrid circuit and also the resulting simulation of the circuit. It could be seen in the simulation as the "blue" signal represents LSB of the two input signals and the green represents the MSB. The resulting signal shows a condition that would fit an AND logic operation. This also applies to the OR logic device in Figure 4. Both of the device also have to be equipped with buffers so the outputs would become more stable.

The principal of the logic design of the 2 memristive logic design would be, when the memristor is positively biased, current will flow through the memristor decreasing the resistance, this is the logic OR configuration. This would also apply the logic AND configuration whereby the polarity of the memristor reversed and the resistance of the memristor would increase. Both logics when have the same input, the output would follow the inputs. While different inputs would have to take consideration of the difference in resistance. Since in OR logic when at different input, it would consider the off resistance, Roff. It would be higher than the on resistance, Ron and due to reverse polarity, logic AND would have opposite resistance as shown in equation 2 and 3 below.

$$V_{out,OR} = \frac{R_{off}}{R_{off} + R_{on}} V_{high} \approx V_{high}.$$

Equation 2: output voltage calculation for OR gate

$$V_{out,AND} = \frac{R_{on}}{R_{off} + R_{on}} V_{high} \approx 0.$$

Equation 3: output voltage calculation for AND gate

After done simulating the previous the two most important design for the full adder, the design is then realized as shown in Figure 4 below
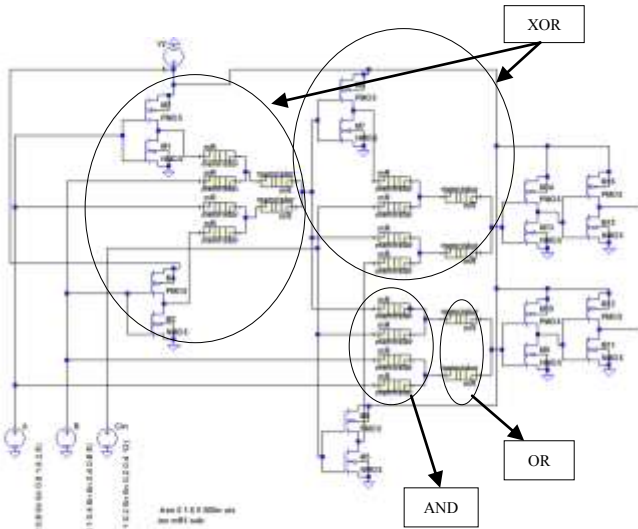
D. Full-Adder

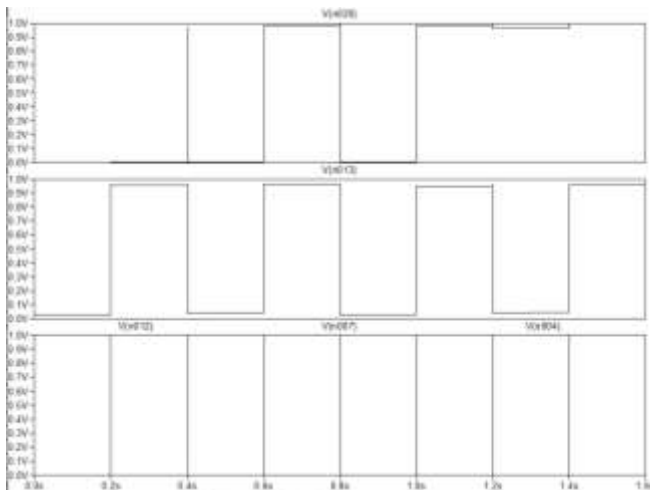Figure 4: hybrid circuit configuration of a full adder device

Figure 5: Output waveform of the hybrid full adder device

It could be seen in Figure 4, the inverter CMOS is used to replicate an XOR logic device. But the desired result did not come out as expected. Figure 5 shows the simulation result of the full adder. The signal from the bottom would be the input signal Cin, B, A, the output signal Sum and Cout respectively. The Cout result was expected while the result was different than the CMOS full adder.

The simulation was analyzed in terms of speed, power consumption and size of the logic OR and AND. The results could be seen in Table 1.

Table 1: Analysis of logic AND OR interms of speed,power consumption and size

		CMOS	Hybrid CMOS
LOGIC AND	Size m^2	2.7x10-13	2x10-17
	Speed CL=50p	0.5µs(2Mhz)	0.8µs (1.25Mhz)
	Power dissipation at 100Ω	0.36µW	0.16µW
LOGIC OR	Size m^2	2.7x10-13	2x10-17
	Speed CL=50p	0.5µs(2Mhz)	0.9 µs(1.11MHz)
	Power dissipation at 100Ω	0.36µW	0.16µW

Basically, the hybrid circuit would have a much lower power dissipation compared to a fully CMOS design and would occupy less space in the design compared to fully CMOS integrated design. In terms of speed, it would lack but could be improved by adding a buffers into the design. By adding buffers to the design, the size would not be overcompensated since the size would still be smaller compared to a fully CMOS integrated design and the speed could be greatly improved since the speed is not much difference when not including buffers.

V. CONCLUSION

As a conclusion, this research could bring familiarization in the integration of memristive components in any kinds of electronic devices that are at nanoscale. The expected results would be that the behavior of the hybrid device which is the CMOS and memristor would give better power dissipation and smaller device. The device could be faster with the addition of buffers without overcompensating the design in terms of speed and power consumption.

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