GeTe Multi-level Phase Change Memory with Separate Heater Layer

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***Abstract*— Phase change memory (PCM) is one of the promising technology for future in non-volatile solid state memory. The concept of phase change memory is the changing state from amorphous to crystalline state. The temperature of changing the amorphous to crystalline is differed according to the phase change material. Ge2Se2T5 is the common phase change material for phase change memory. However the crystalline state for Ge2Se2T5 is (450K-900K). After 900K, the phase change material will melt and become amorphous state. There are few reasons of conducting this project. Firstly, this project is conducting in order to overcome the rapid changes in conventional phase change memory layer which is hardly to control the crystallization process. Then, the implementation of Germanium Telluride and Silicon Carbide (SiC) will be used for the design in order to achieve the multi-level memory. In this project, the phase change memory is designed by using Germanium Telluride as the phase change layer. The top and bottom electrodes for this structure are Titanium Nitride. Then, the heater for this structure is Silicon Carbide and silicon dioxide as the insulator for the structure. The substrate for this structure is Glass (quartz). Figure 1 shows the structure for the design multilevel phase change memory. COMSOL 4.4 will be used for the simulation software. A 100ns SET pulse with time dependent from 0.1 to 3V in order to achieve four bits of multilevel memory.**

Keywords-component; Germanium Telluride, Silicon Carbide, heater, phase change memory, non-volatile memory.

I. INTRODUCTION

Phase change memory (PCM) device is one of the promising device for the replacement of standard floating gate. Generally, phase change memory is simply described as a non-volatile memory device which has the ability to rapidly change from two stable physical states[1]. The states are amorphous and crystalline. During amorphous process, the state of PCM device is in 'reset' whereas the state in crystalline is 'set'[2]. The research of PCM is enhanced over the decades due to high switching mode, low programmable energy, high data retention, and high scalability [3]-[4].

The problem that occur in phase change memory is rapid drop in temperature. When, the set mode is applied to the phase change material layer, the rapid changes of conventional phase change memory is occurred[5]. Due to that, conventional PCM is hardly to control. Thus, the introducing of heater is applied to the PCM device.

In the literature, the data retention that has been proved for PCM is about 10years by using GeSbTe (GST) as the phase change material. For the optimization purpose, Germanium Telluride (GeTe) has been introduced as a phase change material since Germanium Telluride since it is faster compared to the GST [6].Theoretically, the state of GeTe starts from amorphous state which is in scattered state. After the temperature reached at 450K, the state of GeTe will change to the crystalline state until 980K[6].Which mean the period of crystalline is longer than GST.

There are three objectives in this project. Firstly, the using of GeTe as the phase change material in order to achieve the multi-level memory. Then, the understanding of COMSOL 4.4 as the simulation software. The last objective is to obtain 4 bits of multilevel memory

II. METHODOLOGY

Phase change memory or known as PCM is one of the promising device in future. In designing of PCM, there are few computer aided design software that can be used in a simulation. The examples of CAD software are COMSOL and Solidwork[7].

In this project, the CAD software that has been used is COMSOL 4.4. This software is the compatible design since the ability to measure heat, current density and phase change of material are possible.

The initial stage in designing PCM is by selecting the specific purpose or objective for phase change memory. The design starts with by sketching the design using the simulation software. After that, the chosen of the materials have to be right since every materials have the difference preferences. The material that have been used for proposed and conventional design is shown in the table 1.

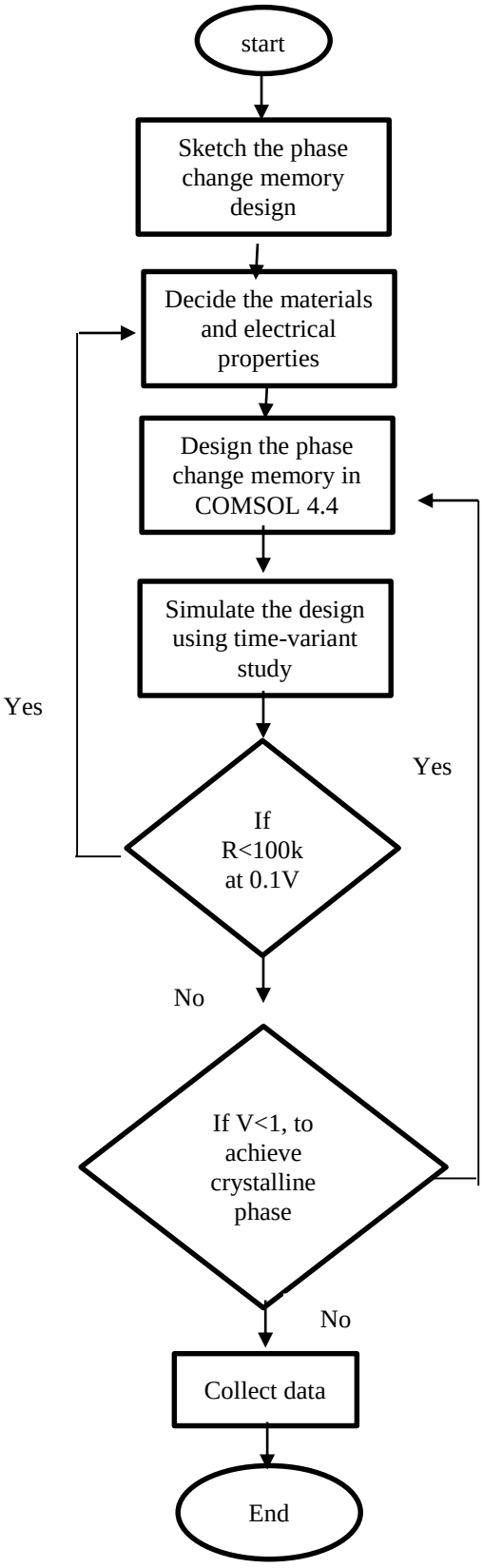

Figure 1. Design flow for the simulation

Figure 1 shows the design flow of phase change memory. The initial stage of designing the phase change memory in COMSOL 4.4 is by sketch and research the design in a hardcopy. Next, the materials and electrical properties of phase change memory have to be decided through the journal or article. This is because some of the electrical properties and materials have to update manually in COMSOL 4.4. In this project, the electrical properties that is used is joule heating. The main elements in joule heating is electrical conductivity, heat capacity, thermal capacity and density[7].

After that, the design is simulated using COMSOL 4.4 in time-variant. The time-variant is the mechanism in COMSOL that allow the designer to set the specified time for the design. In this project, the phase change memory is set in 100ns in order to achieve the objective for this project. If the output resistance is below than 100k in 0.1V, the design need to be rechecked since the concept of phase change memory having resistance drop from high resistance to low resistance. If the result meet the specification or objective for the design phase change, the next step can be proceed which is to collect the data to analyze the design.

Table 1. Electrical properties of materials

Parameter/ material	Electrical Conductivity (S/m)	Heat Capacity (j/(kg*K)	Thermal capacity W/(m*K)	Density (Kg/m)	Size (nm)
Zn-SiO2	0.02	263	0.657	3650	1
SiO2	1e-14	1330	1.4	2330	2
TiN (Top)	5e6	784	22	5240	3
Glass	1e-14	480	1.1	2200	5
GeTe	2.0921e5	260	4.4	6140	10
SiC	4.3e4	1200	450	3200	3
TiN (Bottom)	5e6	784	22	5240	2

Table 1 shows the properties of materials that are using in the phase change memory. There four main importance parameters that have to be emphasized since the project is related to the temperature and current density. The parameters are electrical conductivity, heat capacity, thermal capacity and density.

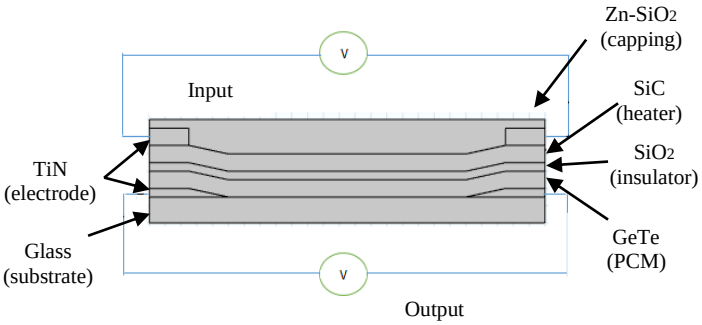

Figure 2. Proposed phase change memory

Based on the figure 2, the structure of proposed phase change memory is started with the top material for the device which is known as capping layer. Next, the design is followed up with top and bottom electrode. The reason of two types of electrode is to classify the electrode as the 'SET' and 'IV' pulses. The voltage for SET pulse is from 0.1-3V. [4]. The material that is used for the both electrodes is TiN.

After that, SiO2 is used as an insulator for the design to avoid direct contact between heater and phase change layer. This will smoothen the flow of heat from heater towards the phase change layers.

Heater that will be used for this project is Silicon Carbide or SiC. Finally, the last material that is used in this design is glass. Glass is used as a substrate for this design.

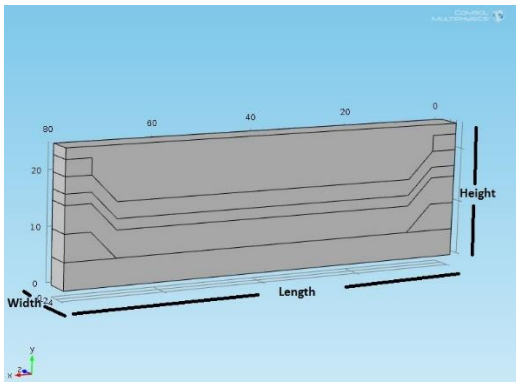

Figure 3. 3D structure of phase change memory

Figure 3 shows the 3D size of the design. The actual design of phase change memory can be seen through COMSOL 4.4. By applying 3D design, the size and thickness can analyzed easily. Thus, this will help to make sure whether the design is in ideal size. By doing 3D design, user able to determine the structure for the design.

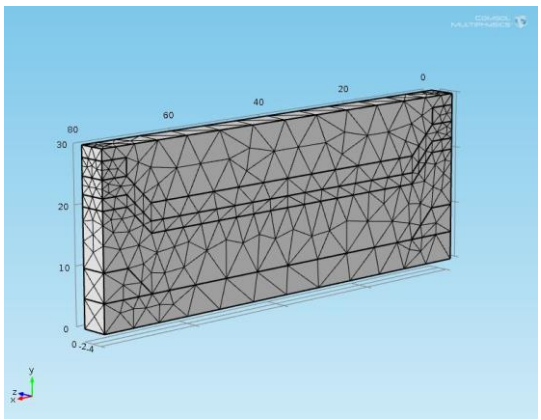

Figure 4. Mesh of phase change memory design

Figure 4 shows the mesh structure of the designed phase change memory. Since phase change memory is the finite element, the implementation of mesh is important. This step will help to ensure the size particle is bonded between the attached materials.

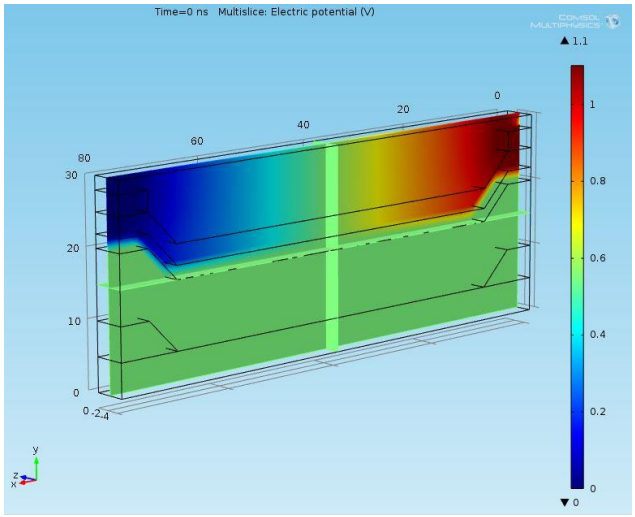

Figure 5. Electric potential in phase change memory

Figure 5 shows the electric potential in phase change memory. The colour of the layer represents the amount of voltage in phase change memory. As the figure __, the current flow from the edge of the TiN electrode to the other side of TiN electrode. These top electrode react as the input for phase change memory. The other electrode that is placed at the bottom of phase change is used to measure the I-V graph and react as the output for the phase memory.

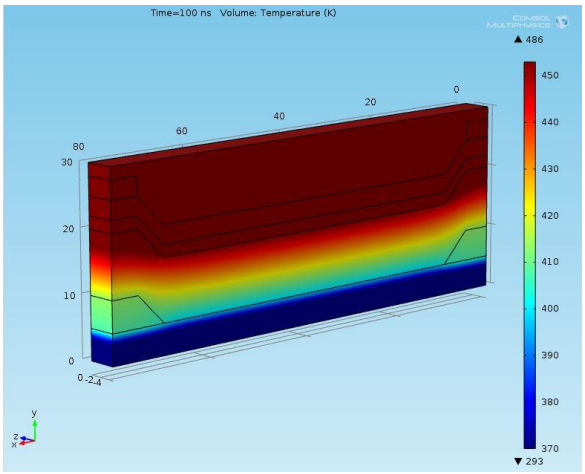

Figure 6. Temperature of phase change material

Figure 6 shows the temperature of phase change memory. Based on the figure, the temperature of phase change is heated at the heater layer. The temperature is lower at bottom part of phase change memory. This is due to the presence of insulator in phase change memory that react as separator between phase

change layer and heater. This will avoid the direct contact between heater and phase change material.

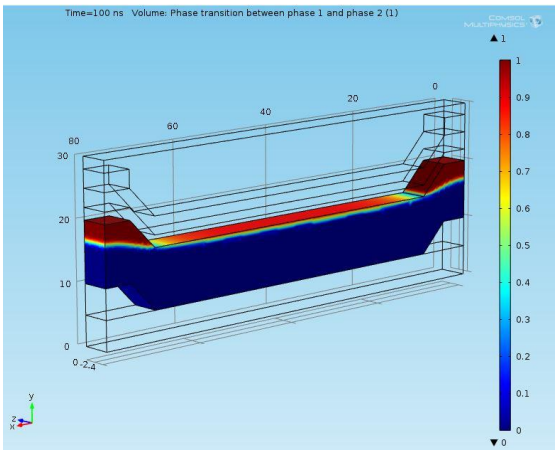

Figure 7. Size phase change of phase change layer

Figure 7 shows the phase change layer of phase change memory. The red colour shows the size of area of phase change memory that has change to crystalline state. The temperature that change the colour of the layer starts from 450K. Thus, the colour of phase change memory will be change to red if all the layer has transform to the crystalline. The temperature will be varied according to the design, size, and materials of phase change layer.

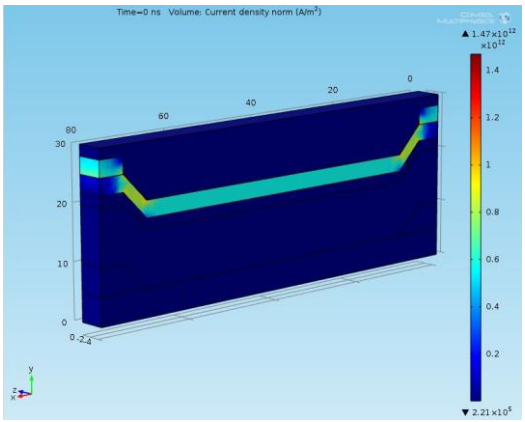

Figure 8. Current density in phase change material

The current density of phase change memory is shown in figure 8. Current density in PCM has to be measured in order to calculate the resistance drop in the device.

This is due to fulfill the concept of phase change memory which has the functionality of multi-level storage. The equation to calculate resistance drop is:-

$$R_{pcm} = \frac{V}{JA}$$

Where;

R_{pcm} : R_{pcm} is the resistance of the phase change memory (kΩ)

V : Applied voltage for I-V, (V).

J : current density, $(\frac{A}{m^2})$

A : area of the phase change layer (m^2)

III. RESULT AND DISCUSSION

In this section, the deep discussion of the conventional design and proposed design will be analyzed and interpreted according to the related influenced subjects. For example, the thickness of phase change layer, structure of phase change memory, effect on applying heater on phase change memory and size. The result and discussion parts have been divided into three categories. Then, 6 stages of SET pulses have been used for this project. These are 0.1V, 0.5V, 1V, 1.5V, 2.0V, 2.5V and 3V.

A. Proposed design Vs Conventional Design.

Part A will discuss and focus on the comparison result between the conventional and proposed designs. Both of the design used the same thickness of memory layer. Memory layer size is 10nm. Both of the designs used similar phase change layer, electrodes and same size of phase change layer.

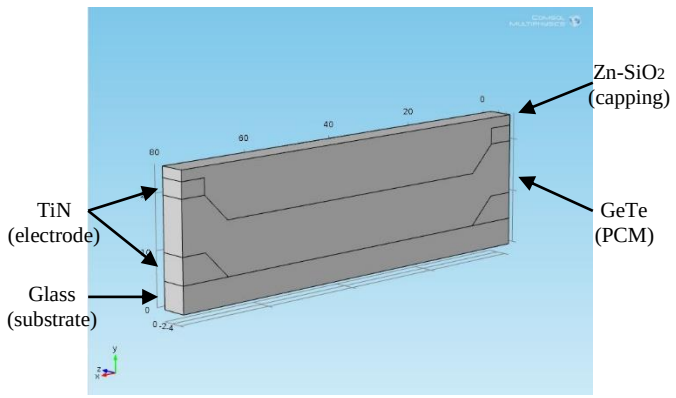

Figure 9. Structure of conventional design.

Figure 9 shows the conventional design of phase change memory.

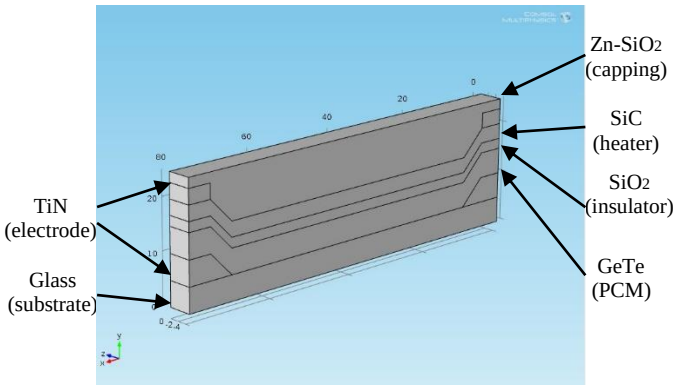

Figure 10. Structure of proposed design.

Figure 10 shows the structure of proposed design of multilevel phase change memory. All the measurement have listed in figure 10.

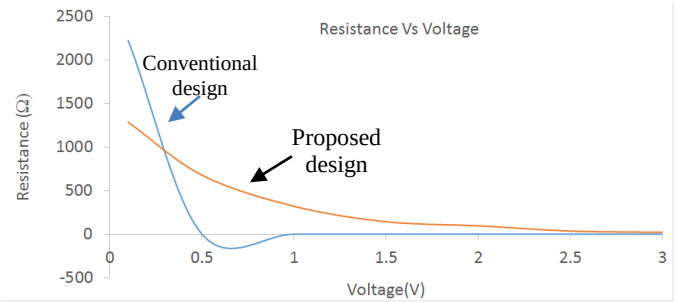

Figure 11. Comparison of resistance drop of proposed and conventional designs

As the result that obtained in figure 11, the resistance drop of proposed and conventional designs are difference in behavior. The initial step for conventional design seems higher compared to the proposed design. However, the resistance drop for the conventional design is drop rapidly compared to the proposed design. The proposed design shows a steadily decline resistance drop.

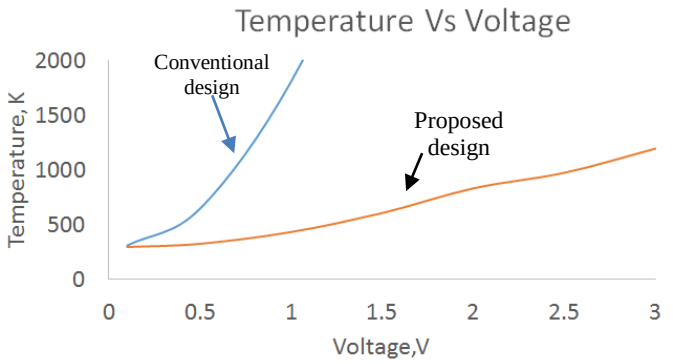

Figure 12. Comparison of rate of temperature of proposed and conventional designs.

Based on the figure 12, the temperature of conventional design reached crystalline phase faster than proposed design. The amount of voltage that required for conventional is less than 0.5V and last before reached 1V. For proposed design, the amount of voltage that required to achieve crystalline phase starts at 1.3V and melted at 2.6V.

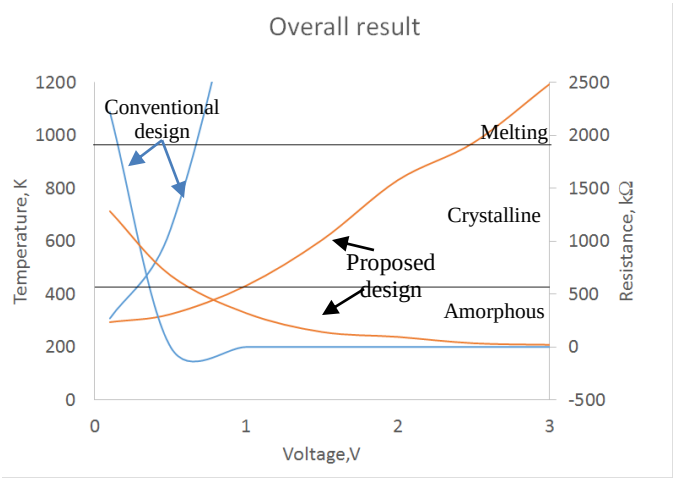

Figure 13. Overall for both designs

Figure 13 shows the overall result for both designs. Based on the results that obtained, proposed design shows a promising result since the duration of crystalline phase is longer compared to the conventional design.

In term of multi-level memory, proposed design can store more bits compared to the conventional. This is because the resistance drop for proposed design decline steadily almost 45 degrees. Thus, the proposed design able to control in four stages which is during 0.8V ,1V ,1.5V and 2V whereas conventional design able to control in one stage which is less than 0.5V.

The factor that lead to this result is the direct contact of top electrode and bottom electrode to the phase change layer. This will excite the temperature rapidly until the phase change reached the melting point at 980K.

B. Width in phase change memory structure

In this part, the subject is focused on the changes of width in proposed phase change memory design structure. The value of thickness is set into five difference values. The values are 5nm, 20nm, 30nm, 50nm, 80nm.

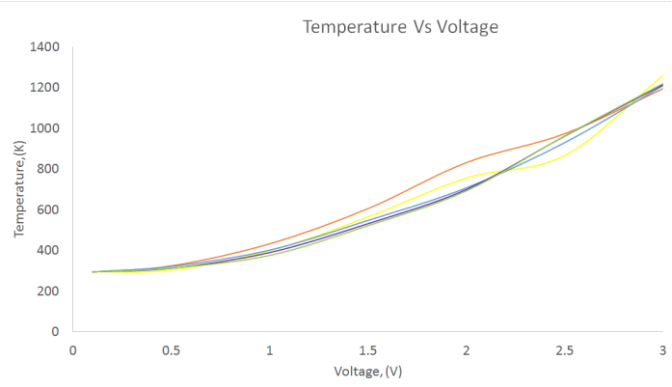

Figure 14: Comparison of temperature in the difference thickness of the structure

Based on the result that obtained from figure 14, the changes of thickness in width do not obviously changes the temperature of the phase change memory.

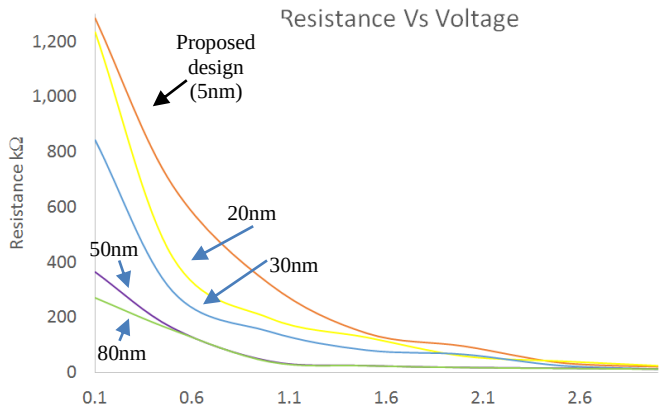

Figure 15. Resistance drop in various thickness in width of proposed design

Based on the result that obtained in figure 15, the width of phase change memory influenced the resistance drop of phase change memory. The small thickness in width of phase change will experience high resistance at the initial voltage. This is because current density for small structure is lower compared to the big structure. Thus, the resistance for smaller width phase change has the potential to hold the amorphous state longer compared to the big width phase change memory[5].

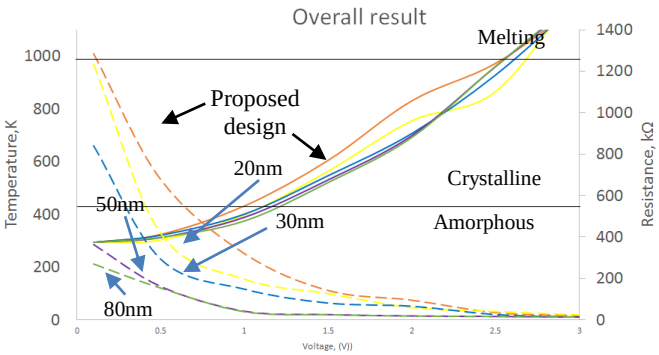

Figure 16. Overall result in difference thickness in width of proposed phase change memory

Based on the figure 16, the overall result of various thickness in width of seemed the proposed design (5nm) is better compared to the other size of the thickness. The crystalline state of proposed design hold longer than other designs. Then, the resistance drop of proposed design is drop steadily following the amount of voltage.

C. Thickness Of Phase Change layer

In this part, the study of thickness of phase change layer is investigated. Five different sizes of phase change layer have decided in order to obtain the ideal size of thickness in proposed phase change memory. Five sizes of thickness have decided in this part. The Sizes are 5nm, 10nm, 20nm, 30nm, 40nm.

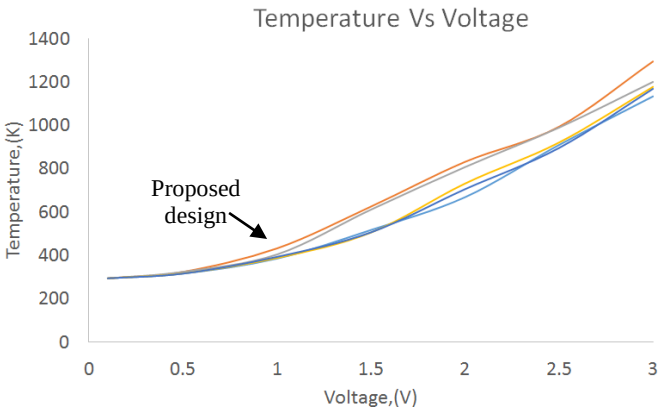

Figure 17. Comparison of the temperature in the various thickness of phase change layer

Based on the figure 17, the temperature does not really influenced by the thickness size of phase change layer. All the designs seem incline steadily with slightly changes.

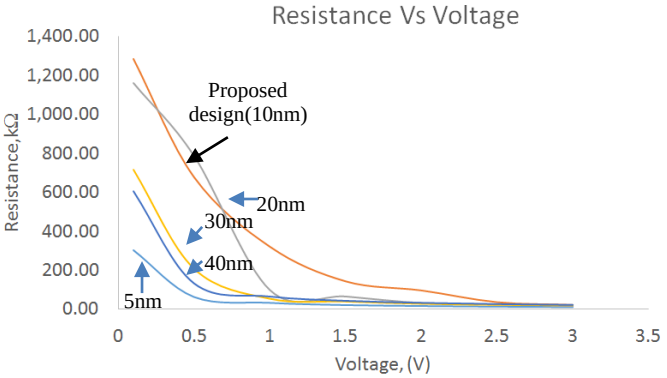

Figure 18. Comparison of resistance drop in the various thickness of phase change layer

Figure 18 shows the comparison of resistance drop in the various size of thickness of phase change layer. The resistance drop is influenced to the size of phase change layer. The resistance drop of thick phase change layer has higher probability in small resistance at the initial voltage. Although, the thin phase change layer is not excluded from having low resistance at the initial voltage. This is due to the non-ideal size of phase change layer.

In 5nm thickness of phase change layer, the size of bottom electrode has the same size as 5nm thickness of phase change layer.

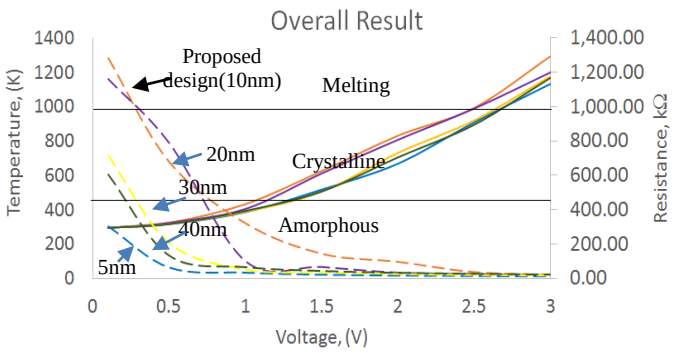

Figure 19. Overall result of the various thickness phase change layer

Based on the figure 19, the overall result for resistance drop and changes of temperature in difference thickness of phase change layer shows 10nm as the best result compared to the other size of thickness. This is due to the decline level of resistance drop is about 45 degrees which is easily to control and succeed the multilevel memory.

The proposed phase change memory able to store bits in 4 stages while the other thickness able to store around one to two bits of memory.

D. Length Of Structure

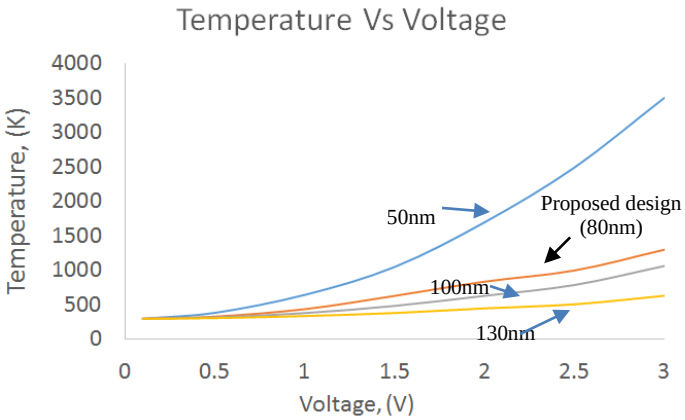

Figure 20. Comparison the temperature of proposed in difference length

Based on the figure 20, the length of phase change layer influenced to the changes of the temperature in phase change memory. The shorter the length of phase change layer, the faster the rate of heat. In designing multilevel memory, lower rate of heat is one of the importance parameter that has to be considered. One of the reason is to avoid rapid changes of state in phase change layer.

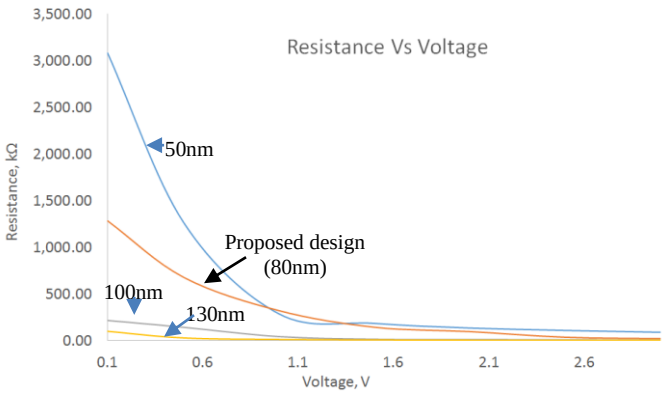

Figure 21. Comparison of resistance drop in the difference of length of phase change layer

Figure 21 shows the comparison of resistance drop in the difference of length of phase change layer. Length is one of the factor that can influenced to the behavior of phase change layer in resistance drop and temperature. Short will experience high resistance at the initial stage. The resistance drop for the short length of phase change layer seems ideal to the concept of phase change memory.

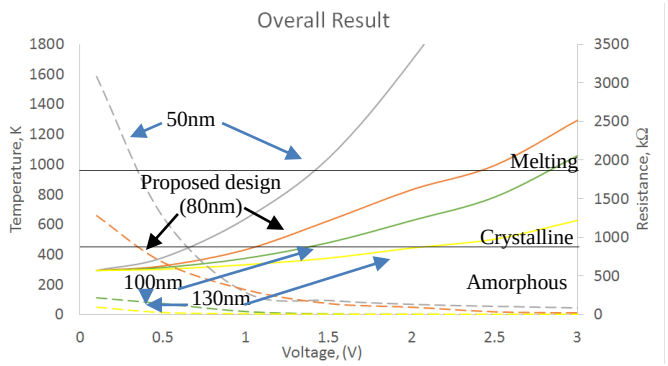

Figure 22. The overall result in the difference of length in phase change layer

Based on the result in figure 22, the overall result shows the ideal size of the phase change layer is 80nm since the resistance drop and the temperature match to be designed as the multilevel memory.

E. Size

Based on the results, the size of structure will influence the resistance drop and changes of temperature. The longer the structure of the design, the rate of increasing in temperature is slower. This is due to the period of heat distribution in phase change material. Then, the thicker the width of the structure, the resistance at the initial period is lower. The thicker the thickness of phase change material, the lower the resistance at the initial period. The ideal size for this project 80nm of length, 10nm of phase change layer thickness and 5nm of width structure.

F. The ability of multilevel memory

The key factor of succeeding the concept of multilevel memory is the ability to change from amorphous state to crystalline state. According to the figure 8, the proposed design incline steadily in temperature to achieve crystalline state. Then, the resistance drop of proposed design drop steadily to the low resistance.[6] Thus, the

IV. CONCLUSION

In a conclusion, the design of phase change memory is achieved the objective. The objective which to design multilevel memory by using GeTe as the phase change material. As the results, the structure of multilevel memory are influenced to the few factors such as length of phase change layer, thickness of phase change layer, width of the structure and the materials. The result is best to clarified according as following:

- Proposed design shows a good result compared to the conventional design.
- GeTe has the ability to perform multilevel phase change memory.
- Separate heater layer and insulator are the most important material that help to prevent rapid changes rate of the temperature and resistance drop.
- The most ideal size for the multilevel phase change memory for this project is 5nm of width, 10nm of the phase change layer thickness and 80nm of the phase layer length.

V. RECOMMENDATION

For further recommendation, there are few suggestions to improve the behavior of multilevel phase change memory. Firstly, using ideal material for the multilevel phase change memory. For example, by applying TiSi3 as the separate heater. Then, the size of phase change layer should be long and thin as possible with current technology. This is because too thin of the structure will cause current leakage for the device. The structure must be suitable with for the current technology which focused towards nanotechnology[8]. Finally, the further study of multilevel phase change memory is recommended in order to achieve the ideal multilevel phase change memory for mass product.

VI. ACKNOWLEDGMENT

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