

DESIGN OF SAP-1 CONTROLLER AND SIMULATION USING MENTOR GRAPHICS

Thesis is presented in partial fulfillment for the award of the
Bachelor of Electrical Engineering (Hons.)
UNIVERSITI TEKNOLOGI MARA



ZAMRI BIN MAJID
Faculty of Electrical Engineering
UNIVERSITI TEKNOLOGI MARA
40450 Shah Alam
Selangor Darul Ehsan
NOVEMBER 1999

ABSTRACT

The control unit of the microprocessor is responsible for providing the necessary timing and control signals to all operations in a microcomputer. One technique for designing microcontrol logic is the microprogrammed control, which derives the sequencing and control logic from the contents of a ROM. This paper presents the design of a microprogrammed control unit for a theoretical computer called the SAP-1 (Simple-As-Possible computer).

The sequencer controller is designed and modeled using the Mentor Graphics Design Architect and QuickSim II package respectively.

ACKNOWLEDGEMENTS

With the name of ALLAH the Most Gracious, Most Merciful alone is worth all praises. I bear witness that there is no god save Allah alone, no partners unto Him, and I bear witness that Muhammad is as his servant and his Messenger, sent him along with the truth, as giver of glad tidings and as a Warner, and to tell that the hour is fast-approaching, no doubt in it. Allah forgives me and straightens me.

I would like to take this occasion to express my gratitude to my project supervisor, Pn. Habibah Bt. Hashim, for her guidance, patience, encouragement, inspiration, support, cooperation and constant guidance has help me to successfully complete the project and this thesis. My appreciation also goes to lecturers and computer laboratory assistants and friends for their willingness to cooperate and assistance throughout the completion of this project. Thank you so much to my family for their support.

MAY ALLAH BLESS ALL OF US.

TABLE OF CONTENTS

CHAPTER	DESCRIPTION	PAGE
	ABSTRACT	i
	ACKNOWLEDGEMENTS	ii
1	INTRODUCTION	1
	1.1 Introduction	1
	1.2 Basic Computer Organization	1
	1.3 Microprocessor Unit	4
	1.4 Timing and Control Unit	6
	1.5 SAP-1 Architecture	7
	1.6 JK Master-Slave Flip-Flop	13
	1.7 Clear-Start Debouncer	17
	1.8 Presetable Counter	17
2	INSTRUCTION SET	20
	2.1 Introduction	20
	2.2 LDA	24
	2.3 ADD	25
	2.4 SUB	26
	2.5 OUT	27
	2.6 HLT	27
	2.7 Memory-Reference Instruction	27
	2.8 Mnemonics	27
3	MICROPROGRAMMING	29
	3.1 Introduction	29

CHAPTER 1

INTRODUCTION

1.1 Introduction

The SAP-1 computer has been designed for the main purpose of teaching the crucial ideas behind computer operation. Its simple architecture allows students to easily understand how a computer works. The SAP-1 computer has been designed with a hardwired controller-sequencer, which sends out control words or microinstruction during each T-state or clock cycle.

The hardwired controller-sequencer can be replaced by a microprogrammed controller-sequencer where microinstructions are stored in a ROM rather than produced by a hardwired control matrix.

The microinstruction required for each instruction and also for the fetch routine can be stored in a control ROM with each instruction routine assigned to a particular address.

In order to fully appreciate the microprogrammed controller designed for the SAP-1, it is necessary to understand the architecture of computers, in particular the SAP-1.

1.2 Basic Computer Organization

Every computer contains the arithmetic-logic unit (ALU), the memory unit, the control unit, the input unit and the output unit as shown in Figure 1.0.