PROGRAMMABLE SAMPLE AND HOLD CIRCUIT FOR RECONFIGURABLE SYSTEM

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ABSTRACT

This project presents a sample and hold circuit design with four different frequency applications such as biomedical signal (16Hz-10MHz), radio frequency (<3kHz-300GHz), intermediate frequency (110kHz-1500MHz) and power (35.9 kHz-90.6 kHz). The frequency applications will be the input to the sample and hold circuit of Silterra CMOS 0.13 μ m technology. The designed sample and hold circuit use 1.5V for the power supply and designed using Mentor Graphic tools. Total power dissipation for sample and hold circuit is 153.89 μ Watts. The variety of frequency applications was used to obtain the different output signal for sample and hold circuit design before the signal is sent to the other system such as an analog digital converter (ADC).

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CHAPTER 1

INTRODUCTION

1.1 OVERVIEW

Reconfigurable system is a system that can change or modified especially sub-system configurations. Reconfigurable devices, including field programmable gate arrays (FPGAs), carry an array of computational elements whose functionality is defined through multiple programmable configuration bits. These components, sometimes known as logic blocks, are plugged in using a set of routing resources that are also programmable. Programmable hardware is the core component in reconfigurable system, and it can be temporary (partly) customized for a specific program or part of the plan. Reconfigurability is divided in two categories:

- i. Static
- ii. Dynamic.