HIGH SPEED WITH LOW POWER FOLDING AND INTERPOLATING ADC COMPARING PERFORMANCE USING TWO TYPES OF COMPARATOR IN CMOS 0.18um TECHNOLOGY

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ABSTRACT

This paper describes the design of a 8-bit CMOS folding and interpolating Analog to Digital Converter (ADC) with high speed comparator. The objective of this paper is to design and identify the performance of the ADC with two type of comparator. Another objective of this paper is to minimize the power consumption of the ADC circuit especially from a comparator. Flash ADC is one of the faster ways to convert any analog signal to a digital signal and use folding and interpolating technique allows each comparator of the ADC to be reused several times over the full scale input range. In addition, interpolating technique can reduce the number of folding circuit required in a folding ADC hence further improve the performance of the ADC in term of capacitive loading and power consumption. Besides that, 60 percent speed of the ADC also depends on the comparator. If we use very fast and stable comparator, the ADC will be more fast and effectively to do the next applications. The simulation results indicate that the Comparator Design 1 achieves low power operation rather than Comparator Design 2 with a minimum number of transistors used, 2GHz of input signal and 497.02mW of power consumption from a single 2V voltage supply based to Gateway SDA tools simulation result.

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CHAPTER 1

INTRODUCTION

1.0 INTRODUCTION

Analog-to-digital converter architecture has become more advanced. Digital clock signal has been incorporated within A/D converter components to meet high-speed design specification. However, digital signal produces much noise and need to be separated from analog circuits which is sensitive to noise. The integration between analog and digital circuit design within a chip introduces mixed signal IC design environment. One of the fastest analog-to-digital converters (ADCs) is the flash ADC. Unfortunately, the number of comparators in a flash ADC grows exponentially with the resolution, requiring excessively large power and area for resolution above 8 bits. However, high speed flash converters can still be realized with the implementation of the folding and interpolating technique and also is an example of mixed signal IC design. However, this architecture exhibits high-power consumption at high output resolution. Due to low power and high-speed conversion requirement for A/D converter, the folding and interpolating architecture is designed. Folding and interpolating ADC uses significantly less comparators and input capacitance then a corresponding fully-flash ADC with equal resolution and hence leads to low power consumption. Moreover, folding and interpolating architecture exhibits the ability to perform high-speed conversion up to one GHz [1] sampling frequency. This thesis describes the design of 8-bit folding and interpolating ADC realized by using TSMC 0.18μm CMOS technology. The ADC is designed to meet certain design specification. The design techniques and issues of folding and interpolating ADC will be further explained in next chapters.