ANALYSIS OF PIPELINE ADC PERFORMANCES WITH DIFFERENT SAMPLE AND HOLD CIRCUITS

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ABSTRACT

This study presents the analysis of pipeline analog-to-digital converter (ADC) with different sample and hold circuit. Pipeline ADC is a device that performs sampling and digitizing of the analog input. The components inside pipeline ADC are sample and hold circuit, comparator, analog adder, gain 2 amplifier and switch. Sample and hold circuit is one of the major contributors to the performances of an ADC. Sample and hold circuit is the most power hungry block that plays a crucial role in pipeline ADC. An appropriate and precise sample and hold circuit is needed in order to optimize the power dissipation of pipeline ADC without affecting its performances. This study focused on the analysis and comparison of the 1 bit pipeline ADC performances using two types of S/H circuits; double buffer S/H and double sampling S/H circuit. The performances of pipeline ADC is measure based on its power consumption and conversion speed. The circuits of pipeline ADC was implemented using 0.18um technology with supply voltage of 1.8V in Silvaco Electronic Design Automation (EDA) tools. Double sampling sample and hold circuit is suitable for pipeline ADC since it consume less power and faster than double buffer sample and hold circuit at high sampling rate or high clock frequency.

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CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

Analog to digital converters (ADC) are extremely vital components in many electronic devices that require interfaces with analog signal and digital signal. ADCs are used in communication applications, voice recorder and medical instruments. Since most of the signals in real world are analog signal such as temperature, sound and audio and microprocessor can only access digital signal, thus, these signals are needed to be converted to digital signal so that it can be read, understand and manipulated by microprocessor.

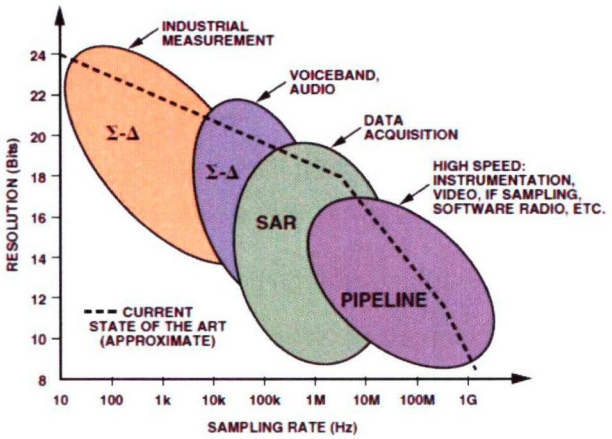

Figure 1.0 Applications, resolution, and sampling rates of ADC [1]