INVESTIGATION OF SHALLOW TRENCH ISOLATION AND SILICIDE EFFECT ON 90NM CMOS DEVICES

This thesis is presented in partial fulfillment for the award of the Bachelor of Electrical Engineering (Honors) (Electronic)

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AKCNOWLEDGEMENT

In the Name of Allah

Most Gracious Most Merciful

Firstly, I like to express my deep sense of gratitude and appreciation toward my supervisor Pn Hanim Bt Hussin for allowing the chance to work under her guidance, opinion and full support in completing this thesis. Without her this work might not be done successfully.

Hereby, I would like to express my deepest thank to my family for their help, support and encouragement in completing this course and thesis.

My sincere and special thanks to all my friends and lecturers especially the member of Semiconductor Devices Lab for the support and providing access required materials for the completion of this thesis.

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May 2010

ABSTRACT

Strained technology is used to enhance the performance of the CMOS that involves physically stretching or compressing the silicon crystal lattice, which in turn increasing carrier mobility without having to make them smaller. Shallow-trench isolation (STI) and silicidation process is the way of strained technology process applied in this investigation. This project discussed on the effect of strain technology on 90nm CMOS device performance focusing on threshold voltage and drain current parameter. Athena and Atlas simulators were used to simulate the process and to characterize the electrical properties respectively. It can be concluded that CMOS with STI and Silicide have better performance than the conventional CMOS. It shows that drain current with STI have been improved by 10% in PMOS and 90.7% in NMOS. While by using Silicide it shows 5.4% in PMOS and 1.82% in NMOS improvement.

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CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

Electronic devices and instruments touch our lives in more than one way these days. They come across as extremely important in many of our daily activities. Their performance, functionality and accessibility define many facets of our daily productivity. The companies designing and manufacturing electronic systems drive whole economies of many parts of the world, both in the developed and developing countries. Thus research and development of better and more capable electronic circuits is an extremely important and continuously growing process ever since the beginning of the electronics age. The electronic revolution involves the discovery of high purity semiconductor materials such as silicon, development of modern fabrication techniques and the development of the integrated circuit (IC) technology.

Moore’s Law states that that the number of transistors that can be placed on an integrated circuit doubles approximately every eighteen months. Downscaling of MOSFETs as standardized by Moore's law is successfully continuing because of innovative changes in the technological processes and the introduction of new materials. Although alternative channel materials with mobility higher than in Si were already investigated, it is commonly believed that strained Si will be the main channel material for MOSFETs. With scaling apparently approaching its fundamental limits, the semiconductor industry is facing critical challenges. New engineering solutions and innovative techniques are required to improve CMOS device performance.

Strain techniques are powerful to enhance performance of modern MOSFETs. It is more economical and quite simple to fit in the modern technological process strain and allows boosting the drive current in both PMOS and NMOS, which is used by the semiconductor industry already, since the 90nm technology node was introduced.