DESIGN AND ANALYSIS OF FULLY DIFFERENTIAL CMOS LNA FOR 3.1-10.6GHz UWB COMMUNICATIONS SYSTEMS

Project report presented in the partial fulfillment for the award of the Bachelor of Electrical Engineering (Hons)

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ABSTRACT

In this thesis, a CMOS Ultra-wideband (UWB) Low Noise Amplifier (LNA) was designed and simulated. In the design, specific architecture decisions were made in consideration. An ultra-wideband (UWB) 3.1-10.6GHz low noise amplifier adopts cross-coupling common-gate (CG) topology is presented in this thesis. Inductive series-peaking is used for the LNA to obtain broadband flat gain in the whole 3.1-10.6GHz band. Designed in a commercial 0.18μm CMOS technology, the LNA achieves an noise figure of 3.1-4.7 dB, an input return loss (S11) of less than -10dB, an S21 of 10.3dB and input 3^{rd} interception point (IIP3) of -5.1dBm, while the power supply is 1.8V.

CONTENTS

CHAPTER 1

INTRODUCTION

1.1 OVERVIEW

The main task of this project is to concentrate on the analysis of optimization of low noise amplifier (LNA) for ultra-wide-band (UWB) communication systems in order to compare the performance with other topologies. The analysis of the circuit will involve simulation in the other words it is very time consuming process.

1.2 PROBLEM STATEMENT

This project is based on software development and the learning outcome is the ability to design the circuit as a basic for optimization and also has the ability to design due to the appropriate applications.

1.3 OBJECTIVE

The objective of this project:

- To use CADENCE as tool for circuit analysis.
- To compare the performance of the UWB circuit as a basis for analysis.
- To design an UWB LNA to achieves good input matching, low noise figure and high linearity.