APPROVAL SHEET

This project report attached here to, entitle "Investigation of Si_3N_4 Capping Layer and Embedded SiGe Effect on 90 nm CMOS Devices" by Norlina Binti Mohd Zain in partial fulfillment of the requirements for the Bachelor of Electrical Engineering is hereby accepted.

This thesis is approved by: Date:

..... 8/5/2010

Mrs. Hanim Hussin

Project Supervisor

Faculty of Electrical Engineering

Universiti Teknologi Mara

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ABSTRACT

This thesis highlights the effect of Si_3N_4 capping layer, embedded SiGe in the source/drain and SiGe layer on the bottom of the strained silicon for strained-silicon technology effect on 90 nm Complementary Metal Oxide Semiconductor (CMOS) performance focusing on threshold voltage and drain current parameters. Strained silicon is used to increase saturated NMOS and PMOS drive currents and enhance electron mobility. Compressive strain is introduced by two techniques strained in the PMOS channel using SiGe such as uniaxial strained and biaxial strained. Tensile strain is introduced in the NMOS channels by using a post silicon-nitride capping layer. ATHENA and ATLAS simulators were used to simulate the fabrication process and to characterize the electrical properties respectively. It can be concluded that NMOS strained technology having high tensile stress improve by 46.9% drain current. PMOS strained technology having compressive stress using biaxial strained PMOS improve 16.4% while uniaxial strained PMOS improve 21.4%. The strained technology were the best on 90 nm for CMOS device is combination of Si_3N_4 film tensile strain for NMOS and uniaxial compressive strain for PMOS.

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CHAPTER 1

INTRODUCTION

1.1 BACKGROUND OF STUDY

According to Moore's Law, Sir Gordon Moore predict that the number of transistor is going in the trend of doubling every two years. Due to the increasing number of transistor in a chip, thus each transistor size is decreasing geometrically, reducing the cost yet increase the speed.

After more than three decades of continued progress in CMOS devices technology, especially aggressive scaling in the last few years, the CMOS scaling is now approaching the fundamental limits. In the nanometer regime, stress from standard process steps such as source/drain doping introduces significant stress in the channel of MOSFETs. With the continuing reduction of device dimensions, the impact of process-induced stress on device performance is becoming increasingly important. Besides scaling, several innovative mobility enhancement techniques are being attempted to maintain the CMOS performance improvement.

Mobility enhancement is important to improve the device performance without performing device scaling. It has been shown that the introduction of a compressive and tensile stress in the silicon (Si) channel can improve the mobility hole and electron and in turn increase the n- and p-MOSFET drive currents.