POWER EFFICIENT 64-BIT DYNAMIC COMPARATOR USING 0.18µm TECHNOLOGY

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Thesis presented in partial fulfillment for the award of the

Bachelor of Engineering (Hons.) Electronics Engineering

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CANDIDATE'S DECLARATION

It is hereby declares that all materials in this thesis are the results of my own work and all the materials which are not the results of my own work have been clearly acknowledge in this thesis. Although, certain result on this thesis is effort from other dispute.

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Date:

DEDICATION

Dedication in thankful appreciation for support, encouragement and understandings

to:

My project supervisor, Puan Lailatul Bt Hassan

My Beloved mother, and father, Mohd Zaidi bin Abdullah;

Also my beloved friends Suhaib bin Tarmizi, Jared ak Jahari, Muhd Syafiq bin Abdul Rahim, Hasliadi Guliga, Azrin bin Wasli and Nor Elyna bt Abdul Wahab.

And all people contribute to this project.

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Last but not least, to my family for giving me encouragement and morale support, they also provide me financial support that I need most upon complete this project. I also like to thank all of my friends for their comment, helps and courage.

Thank you very much and may Allah bless you always.

ABSTRACT

This thesis presents the comparative study on 64-bit dynamic comparator using 0.18µm CMOS technology. The objective of this thesis is to study and compare the speed of the comparator using 0.5µm and 0.18µm technology and to compare the power consumption/dissipation for comparator in 0.5µm and 0.18µm technology. Comparator is a device that compares two inputs and chooses the high/low or same value to be the output depends on the device application. The tools used in designing comparator are SILVACO GATEWAY for schematic design. Result show that the power consumption are 3.81nW and the delay is 142.98ps.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

ABBREVIATIONS

CMOS	- Complementary Metal-Oxide Semiconductor
ADC	- Analog Digital Converter
EDA	- Electronic Design Automation
IC	-Integrated Circuit
RAM	-Random Access Memory
V_{DD}	-Voltage supply
GND	- Ground
MOSFET	- Metal-Oxide Semiconductor Field-Effect Transistor
NMOS	- Negative Metal Oxide Semiconductor
PMOS	- Positive Metal Oxide Semiconductor
TTL	-Transistor-transistor Logic
VLSI	-Very Large Scale Integration
μm	- micro meter
nm	- nano meter

CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

This thesis presents two topologies of dynamic comparator that is equality comparator and zero/one comparator. The purpose is to design the power efficient 64-bit dynamic comparator using 0.18µm CMOS technology. The main parameters that been evaluated are speed and power. This is because the target of this project is to design power efficient comparator using 0.18µm and 0.5µm and comparing the speed between 0.18µm and 0.5µm technology. Power efficient means it must have a low power or even power even the speed is increased.

This project is based on the fast dynamic 64-bit comparator with small transistor count journal [1] that and been proposed in the technical paper of Power Efficient 64-bit Dynamic Comparator Using 0.18µm Technology.

1.2 BACKGROUND STUDY

Comparator is a device use to compare between two inputs and select one output depends on the device application. There are many types of comparators such as voltage comparators, current comparators, latch comparators, dynamic comparators and etc. Different comparators have different functions. ADC is an example of devices that using comparator.

Speed and power consumption/dissipation are the main parameters that need to be concerned when designing the comparator. The ever-growing application of portable devices makes the power consumption a very critical constraint for circuit designers [2]. Comparator is the simplest circuit use to convert analog or digital to create

relevant outputs [3]. Technology chose also one of the factors that affect the delay and power consumption of the comparator.

Comparators are used in central processing units (CPUs) and microcontrollers (MCUs). High-speed operation has always been a target in circuit design because of the speed demand for technology today [2] .A critical operation in comparator is the comparison of two binary input data.

This thesis compares the simulation result between the proposed designs of 0.18µm technology with the reference paper using 0.5µm technology, which will minimize the delay and the power consumption of the comparator. So, the comparator will be more sensitive and comparing speed tends to be fast

1.3 PROBLEM STATEMENT

The problem for existing comparator is the speed and the total power consumption/dissipation. The speed and power consumption/dissipation of existing still can be improved. To improve the speed, the new design comparator must reduce the delay so the speed becomes faster. To improve the comparator speed, different technology CMOS is used. Technology chosen for this project is 0.18µm CMOS technology to be compared with the previous technology that using 0.5µm technology. This research needed to minimize the delay for the comparator and power consumption/dissipation of the comparator. SILVACO EDA tool is used for designing the schematic circuits and for the simulation of the design.

1.4 SIGNIFICANCE OF THE STUDY

1. The design of this project will give a smaller delay than the studied reference paper [4], using CMOS 0.5µm technology.

2. Introduce the design topology of equality comparator and zero/one comparator [4], which is used as a proposed schematic design.

3. This project will minimize the delay and the power dissipation of the comparator. So, the comparator will be more sensitive and comparing speed tends to be fast.

1.5 OBJECTIVES

The objectives of this project are:

1. To study and compare the speed of comparator chosen using 0.5µm and 0.18µm technology.
2. To study and compare the power dissipation of comparator chosen using 0.5µm and 0.18µm technology.
3. To design schematic using SILVACO EDA tools.
4. To obtain the transient analysis results using SILVACO EDA tools.
5. To compares the different between 0.5µm and 0.18µm technology in SILVACO EDA tools.

1.6 SCOPE OF WORK

The scope of this project is to design a power efficient 64-bit dynamic comparator using 0.18µm technology. Power efficient comparator must have a low power and small delay. In order to achieve the expected results, smaller CMOS technology is used. 0.18µm CMOS technology is used in this project and to be compared with 0.5µm CMOS technology. To get smaller delay, smaller width and length for transistor is required. So, the width and the length must be different between the two technologies. The results obtained by using SILVACO EDA tools and then compared with previous work [1].

1.7 THESIS ORGANIZATION

This project report consists of five chapters. Each chapter discussed details of the particular topic in order to provide good understanding on this work.

Chapter 1: covered the introduction of the basic idea of this project, problem gathered from the investigation, the objectives to improve the existing project and the scope of the work.

Chapter 2: discussed the literature review about the studied reference paper[1]. This chapter also described the method used and the reason it is chosen based on the design specs.

Chapter 3: details the concept and method used to complete this project from the initial phase until the final stage. The details include the flow charts, block diagram, circuit design, and the techniques used.

Chapter 4: shows the results obtained from this work as well as presenting the discussion. The discussion is achieved by comparing result obtained with the expected result and reference paper studied. The problem occurred also discussed in this chapter.

Chapter 5: presents the conclusion of the overall result and suggestion for the development.

CHAPTER 2

LITERATURE REVIEW

2.1 INTRODUCTION

All information and knowledge about the dynamic comparator, equality comparator and zero/one comparator were collected. Then the procedure of designing power efficient 64-bit dynamic comparator was identified. A research has been done to recognize the best way to produce the smaller delay and low power dissipation for the comparator. In this chapter, a brief explanation about the comparison between studied reference paper and the idea used to create and develop new idea that meets the objective of this project are discussed. This project is based on the technical paper of Low Power CMOS Dynamic Latch Comparators [1] which proposed two comparators topologies. The equality comparator and zero/one comparator joined to become a dynamic 64-bit comparator. Then, the technologies for these comparators are change using 0.18µm and 0.5µm technology.

2.2 CMOS

CMOS is a technology used for manufacturing IC's. CMOS technologies are commonly used in digital logic circuits, RAM, microcontrollers and microprocessors. In 1967, Frank Wanlass patented CMOS (US patent 3,356,858)[4].

CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors, MOSFETs for logic function [4]. The CMOS circuit design process consists of describing circuit inputs and outputs, hand calculations, circuit simulation, circuit layout, simulation input and output, fabrication and testing.

The focal principle behind CMOS circuits is used of p-type and n-type MOSFET to create paths to the output from either VDD or GND. It said to be pulled up, when a path output is created from the voltage source while pulled down when a path output created from the ground of the circuit.

Gordon Moore observed in 1965 that plotting the number of transistors that can be most economically manufactured on a chip gives straight line on semi logarithmic scale [5]. Transistor was found that it could be doubling every 18-month. This observation has been called Moore's Law. From this law, it is important to reduce the size of transistor and design the smaller chip but make sure the design produce low power and high-speed operation.

Low static power consumption and high noise immunity are two main features of CMOS devices. The series combination draws substantial power temporarily during the switching between on and off state since one of the transistors of pair is always off. CMOS devices such as TTL and NMOS do not produce as much excess heat but typically have some standing current when not changing state. CMOS became the most used technology to be applied in VLSI chips because it's allows a high density of logic functions on a chip.

2.2.1 MOS GATE

MOS gate consist three pins, which is gate, drain and source. The gate of a MOS transistor controls the flow of current between drain and source. Length and width of that active on the transistor is control by gate [6]. Figure 2.1 shows the NMOS and PMOS transistor.

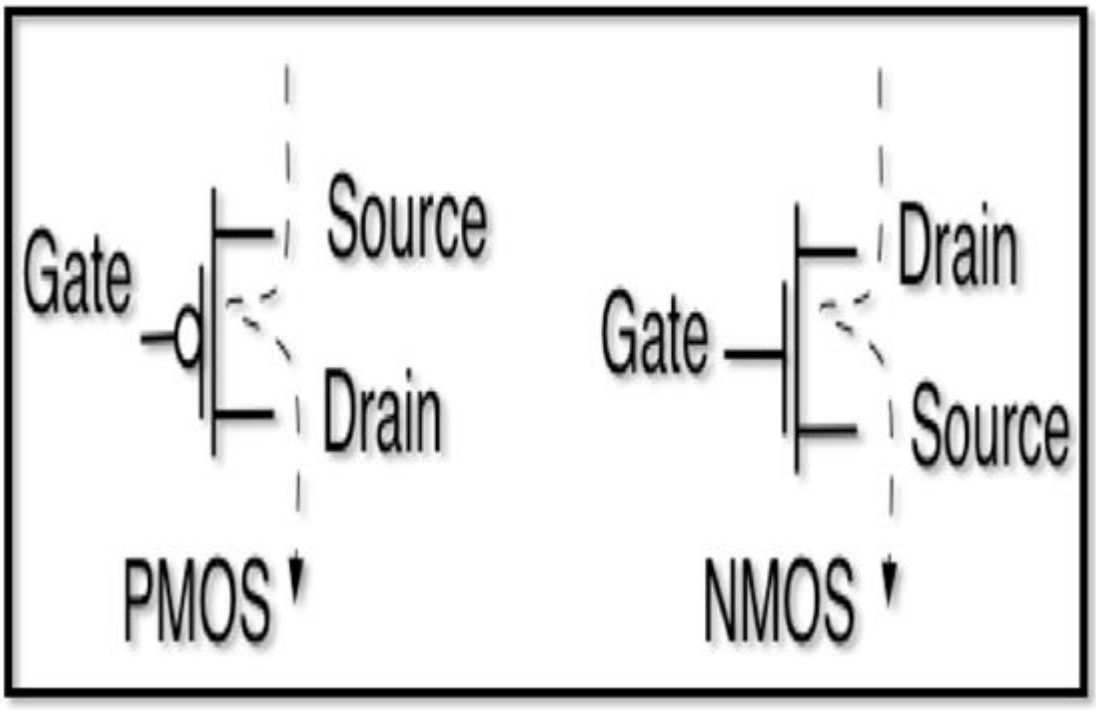

Figure 2.1: NMOS and PMOS symbol

When designing CMOS circuit, widths of PMOS transistor are double than width of NMOS. This is because the majority carriers of PMOS are electrons, which is half of the speed of the holes, which are majority carriers of NMOS transistor of same size. It make PMOS is slower than NMOS. So, in order to have both same speeds, the size of PMOS size must be double of the NMOS size.

2.2.2 MOS OPERATION

Logic gate can be created using NMOS and PMOS transistor. A simple MOS operation can be show in Figure 2.2. Inverter is an example of simple MOS operation. The power supply, VDD (5V) and GND is assumed as logic 1 and logic 0. Inverter is a series connection between NMOS and PMOS. These transistors are connected between VDD and GND.

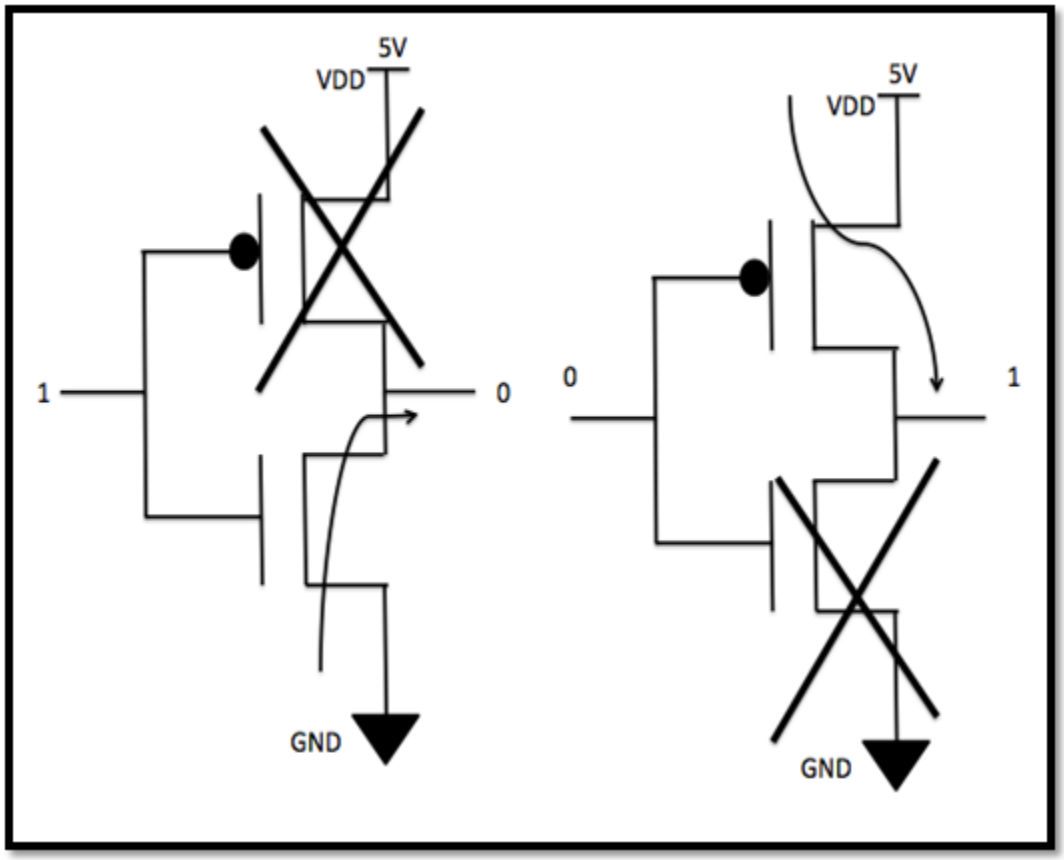

Figure 2.2 Inverter operations

When input is 1, the NMOS is conducting while PMOS is not and in OFF state. So, the output is 0. When the input is 0, the PMOS is conducting while NMOS is not and the output is 1.

2.3 LOW POWER DISSIPATION

A major innovative challenge nowadays circuit designers are to design new products, which consume minimum power in many ADC, especially those used in portable device that have limited power supply energy [3]. Low power consumption and high speed is important feature of many ADC design to reduce energy use or to minimize heat dissipation to lower cooling and packaging costs. Power saving must be achieved without compromising high performance or minimum area [7]. The reasons of designing the low power are to reduce the energy use, minimize heat dissipation and save the cost of product.

One way to reduce the power dissipation is to reduce the power supply voltage. However the delay increases significantly, when VDD approaches the threshold voltage. To overcome this problem, the devices should be scaled properly. The advantage of scaling for low-power operation is improved device characteristics for low voltage operation due to improvement of the current drive capabilities [7].

2.4 COMPARATOR

Comparator is a special combinational circuit use to compare two inputs/magnitude and the output are A=B, A<B or A>B [1]. The comparator chose the high value or low value as the output depends on the inverting or non-inverting inputs that trigger the output to be chosen according to the circuit needed.

Comparator is the simplest circuit use to convert analog or digital to create relevant outputs [2]. Several parameters needed to be considered when designing the comparator such as width and length of the transistor; the speed, power consumption and chip area are the important factors while designing comparators [2]. Technology chose also one of the factors that affect the delay and power consumption of the comparator.

Comparators are used in central processing units (CPUs) and microcontrollers (MCUs). High-speed operation has always been a target in circuit design because of the speed demand for technology today [3]. A critical operation in comparator is the comparison of two binary input data. Theoretically, the fastest comparator is made of full combinational logic gates. NMOS and PMOS transistors of static CMOS gate are dual of each other; one of them will always be arranged in series. These transistors will increase the loading seen by the previous stages.

2.5 DIGITAL COMPARATOR

AND, NOR and NOT gates are standard gates that used to create digital comparators. Digital signals present are compared at their input terminals and the output produce depends on the inputs conditions. Digital comparator operates using the Boolean algebra principles. There are two types of digital comparator, an identity comparator

and magnitude comparator. Identity comparator is a digital comparator that has one output terminal such as A = B or A<B or A>B. for magnitude comparator, it has three output terminal that consist A<B, A=B and A>B. Figure 2.3 shows the example of the 1 bit digital comparator

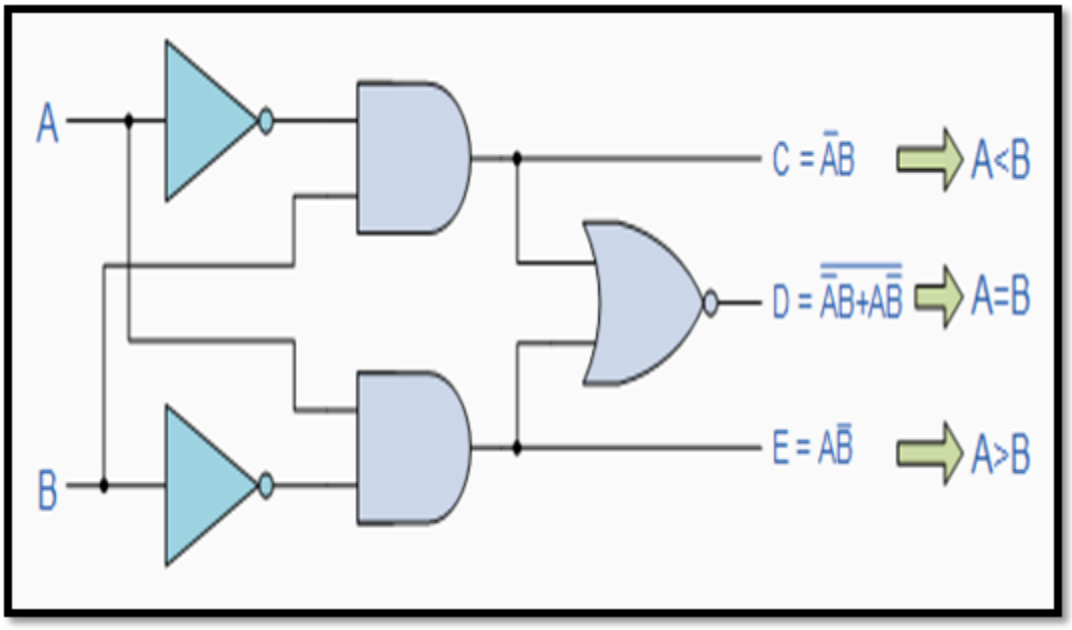

Figure 2.3: 1 bit digital comparator

A journal wrote by Mohammad Larijani and Mohammad bagher Ghaznavi-Ghoushchi presents a new digital comparator based on the general form of the n-bit digital comparators with majority functions. This study used 64-bit digital comparator built on the top of a modified and improved Domino Logic with pipeline structure. The design is without the inter-block inverters of the conventional domino logics. The proposed comparator is evaluated in 90nm at 1.2v VDD at clock frequency of 4.2GHz with 1.2-clock cycle delay or 310 picoseconds and The power and Power-Delay Products in 90nm are 3.3mw and 1.12pJ respectively. The design is evaluate with 90nm PTM (Predictive Technology Model) at the clock rate of 5.4GHz or about 50% improvement against the best-known previous digital comparator to show the effectiveness. Moreover, the design is simulate in AMI (Algorithmic Modeling Interface) 0.5um at 5v VDD shows 2.0 GHz clock speed and 1.5 clock cycle delay or

750 picoseconds. As the result, it shows about 43% improvement against the best-known digital comparator using this technology [8].

A journal wrote by Saleh Abdel-Hafeez, Ann Gordon-Ross and Behrooz Fahrami present a new comparator design using only conventional digital CMOS cells that introduced wide-range and high-speed operation. This comparator exploited the original scalable parallel prefix structure. When the compared bits are equal, the comparator leverages the comparison outcome of the most significant bit, proceeding bitwise toward the least significant bit. This method eliminated unnecessary transitions in a parallel prefix structure that generates the N-bit to reduce dynamic power dissipation by comparison result after ⌈log4 N⌉ + ⌈log16 N⌉ + 4 CMOS gate delays. This comparator composed of interconnected CMOS gates with a maximum fan-in and fan-out of five and four. The main advantages of this design are high speed and power efficiency, maintained over a wide range. This design uses a regular reconfigurable VLSI topology, which allows analytical derivation of the input-output delay as a function of bit width. HSPICE simulation for a 64-b comparator shows a worst-case input-output delay of 0.86 ns and a maximum power dissipation of 7.7 mW using 0.15μm TSMC technologies at 1 GHz [9].

A journal entitled 1GHz 64-bit high-speed comparator using ANT dynamic logic with two phase clocking has been published. This journal presented about a high-speed 64-bit comparator using ANT dynamic CMOS logic with modified non-inverting all transistors N-block. Inserting two feedback MOS transistors between the evaluation N-block and the output accelerates the pull-up charging and pull-down discharging of a comparator unit. A parallel tree structure with two-phase clocks is employed to increase throughput. The comparator units of two adjacent layers are triggered by two out-of-phase clocks so that their individual outputs are pipelined without using extra hardware e.g. latches. The operating clock frequency is 1.0 GHz while the compared output of two 64-bit binary numbers is done in 3.5ns [10].

A published journal shows the study of several design techniques for high-performance and power-efficient CMOS comparators. First, the comparator is based on the priority-encoding (PE) algorithm, and the dynamic circuit technique developed specifically for the priority encoder can be applied. Second, the PE function and the subsequent logic functions are merged and efficiently realized in the multiple output domino logic (MODL) to result in a shortened logic depth. The circuit in MODL CMOS is also compact and power efficient because few transistors are needed. Third, the multilevel look-ahead technique is used to shorten the path of priority-token propagation. Finally, the circuit is realized with a latch-based two-stage pipelined structure, and the comparison function is partitioned into two parts, with each part executed in each half of the clock cycle in a delay-balanced manner. Post-layout simulation results show that a 64-b comparator designed with the proposed techniques in a 3V 0.6μm CMOS technology is 16% faster, 50% smaller, and 79% more power efficient as compared with the all-n-transistor comparator, which is the fastest among the conventional comparators. Measurement results of the test chip conform with simulation results and prove the feasibility of the proposed techniques [11].

In a journal wrote by Chua-Chin Wang, Ya-Hsin Hsueh, Hsin-Long Wu and Chih-Feng Wu, it propose a 64-bit fast dynamic CMOS comparator with small transistor count. The proposed comparator are the rearrangement and re-ordering of transistors in the evaluation block of a dynamic cell is the major features, and the insertion of a weak n feedback inverter helps the pull-down operation to ground. The simulation results given by pre-layout tools, e.g. HSPICE, and post-layout tools, e.g. TimeMill, reveal that the delay is around 2.5 ns while the operating clock rate reaches 100 MHz. A physical chip is fabricated to verify the correctness of our design by using UMC (United Microelectronics Company) 0.5μm (2P2M) technology [1].

2.6 EQUALITY COMPARATOR

An equality comparator is not a magnitude comparator. It has an output only show A = B. Example of inputs and output shown in Table I. When A = 1 and B = 1, output will be set active showing that A = B. Same case also applied when input A = 0 and B

= 0 but when input A = 0 and input B = 1 or vice versa, output will show 0 showing that A not equal to B. Example of equality comparator can be shown in Figure 2.4 [1].

Table 2.1: Truth table of 2 input equality comparator

INPUT		**OUTPUT**
A	**B**	**A = B**
0	0	1
0	1	0
1	0	0
1	1	1

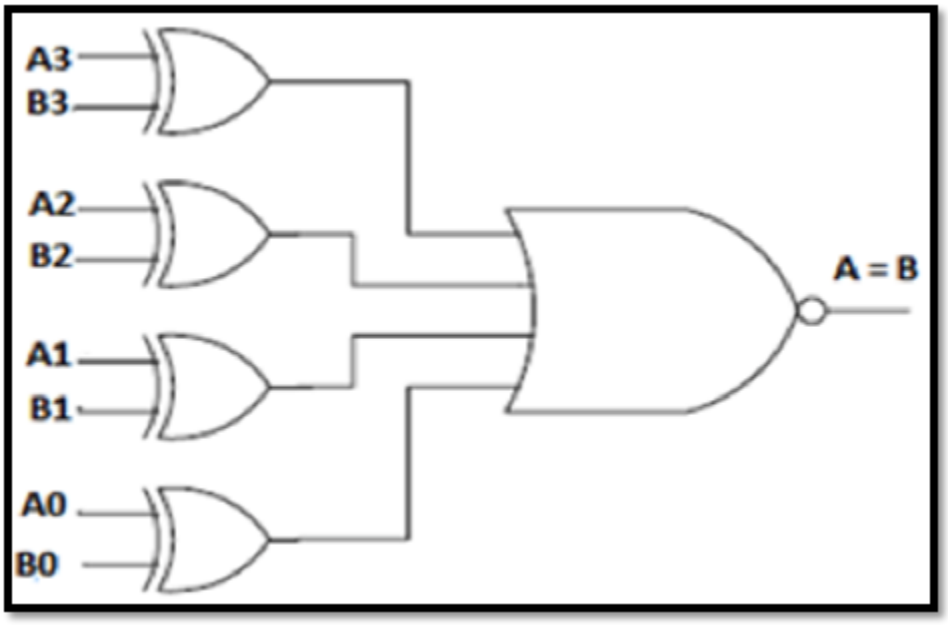

Figure 2.4: Equality Comparators

A published journal in year 2004 proposed equality comparator (EC), which exploits the fact that unequal cases happen more frequently in compare operations. Conditional pseudo-NMOS NAND gates save the power of the unused sub-ECs. The proposed EC-I in this journal delays is 0.857ns and the average power of 1.522mW. For the proposed EC-II, the delays are 1.214ns and the average power is 0.939mW.

The proposed 64-bit EC results in 31% faster speed and 42% less power dissipation than the conventional dynamic EC [12].

2.7 ZERO/ONE COMPARATOR

Zero/one comparator is a comparator detects each time an AC pulse changes polarity. The output of the comparator changes state each time the pulse changes its polarity, that is, the output is HIGH for a positive pulse and LOW for a negative pulse squares the input signal.[13]. Figure 2.5 shows the example of zero/one comparator circuit's design using gates [1].

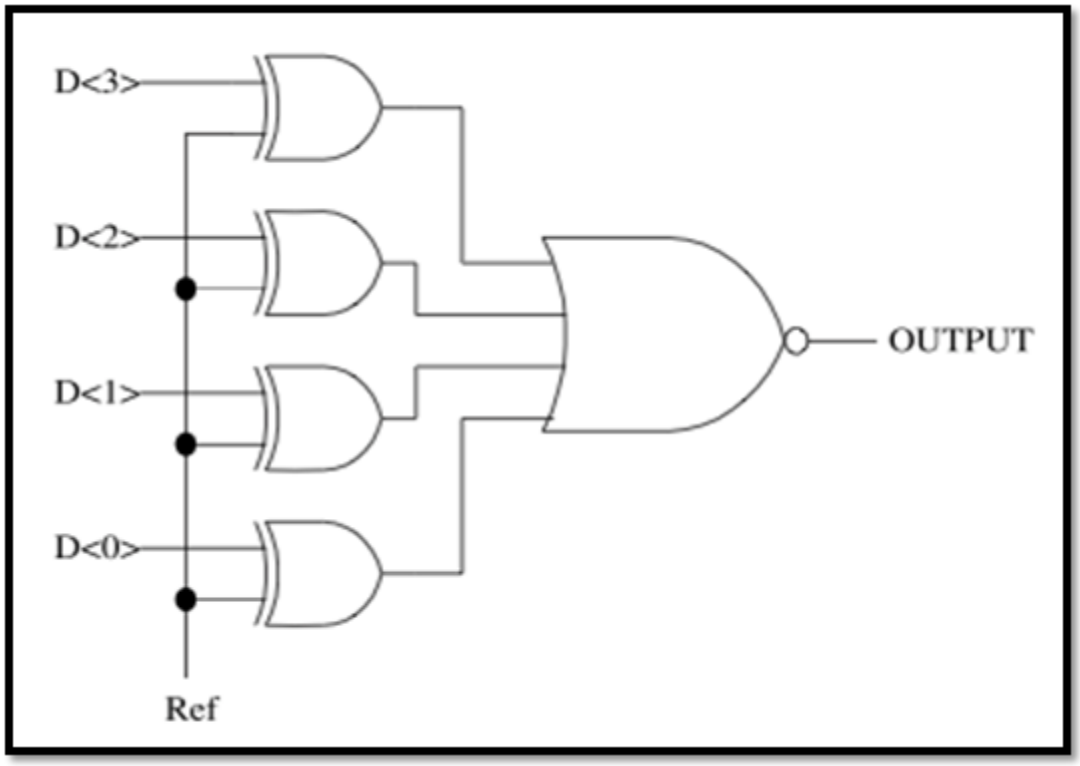

Figure 2.5: Zero/one Comparators

CHAPTER 3

METHODOLOGY

3.1 INTRODUCTION

In Methodology chapter, all of the processes involved to complete this project are discussed. It includes the workflow of the project; procedure involved in designing comparator circuits using SILVACO EDA Gateway, block diagram of the comparator and the testbench circuit.

3.2 WORKFLOW OF THE PROJECT

Methodology is an analysis principle of method used in this project to ensure the successfulness of the project done. This project is done by researching the literature review of the project including the reference that cover within the scope of work and study and also analysis on the work that had done before. It is summarized in the diagram below. Figure 3.1 below shows the overall flow of the project.

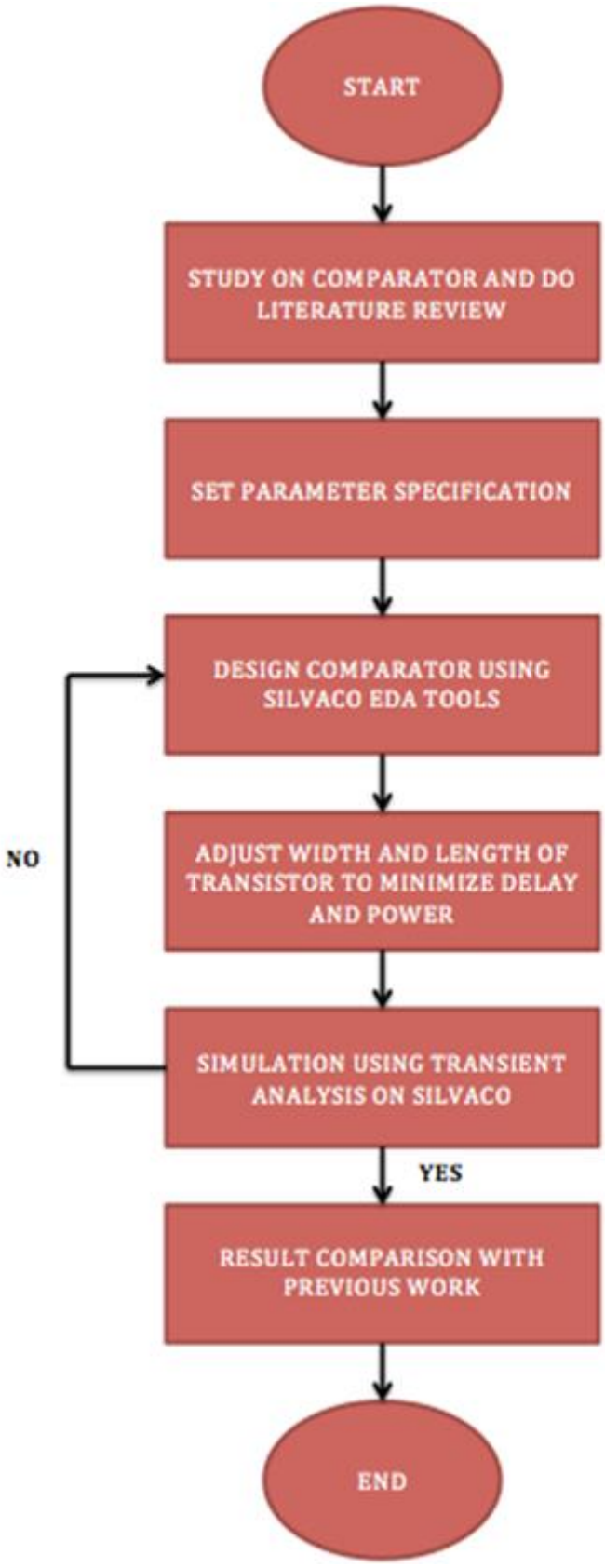

Figure 3.1 Flowchart of the project

3.3 DESIGN TOOLS

The design tools used in this project is SILVACO EDA tools. SILVACO EDA Gateway is use to design schematic circuit. Figure 3.2 shows the SILVACO EDA Gateway that used to design schematic circuit. Gateway is a powerful schematic capture and editor functionality to create and modify multi-view, multi-sheet hierarchical IC designs. It also connected with Smart spice editor that used to show the waveform after the simulation is done. SILVACO EDA Gateway also has DC bias display for current and voltage throughout hierarchical. Figure 3.3 shows the smart spice waveform after the simulation using transient analysis.

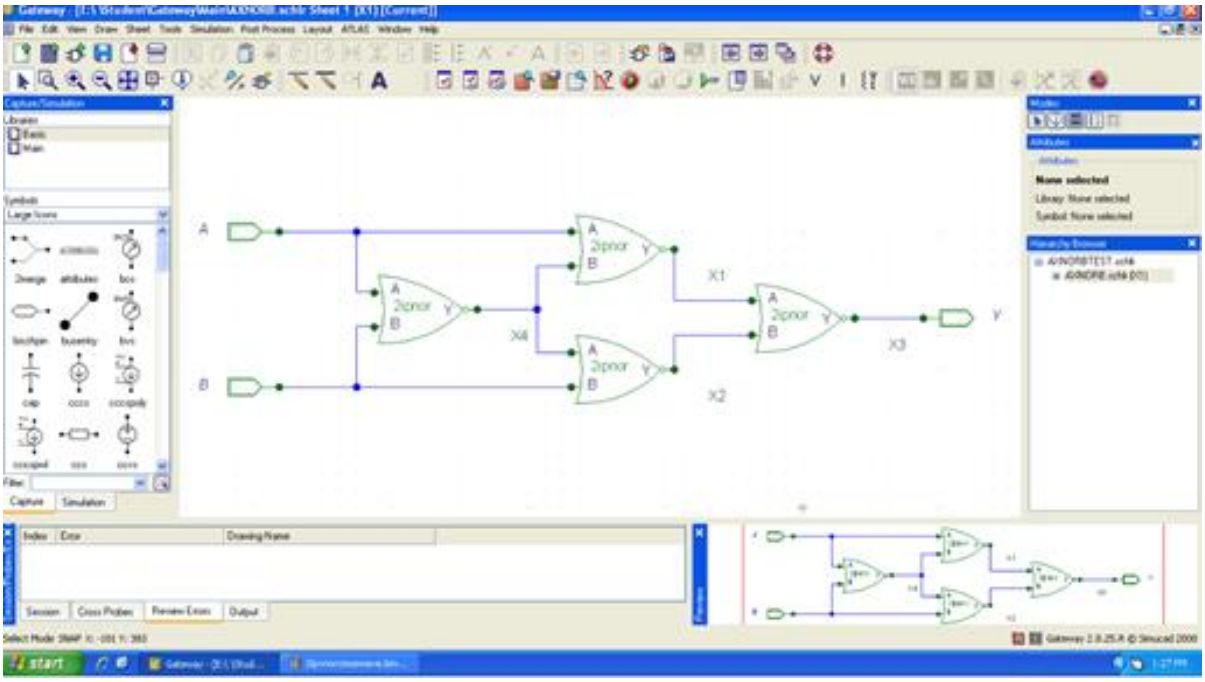

Figure 3.2: SILVACO EDA Gateway Tools

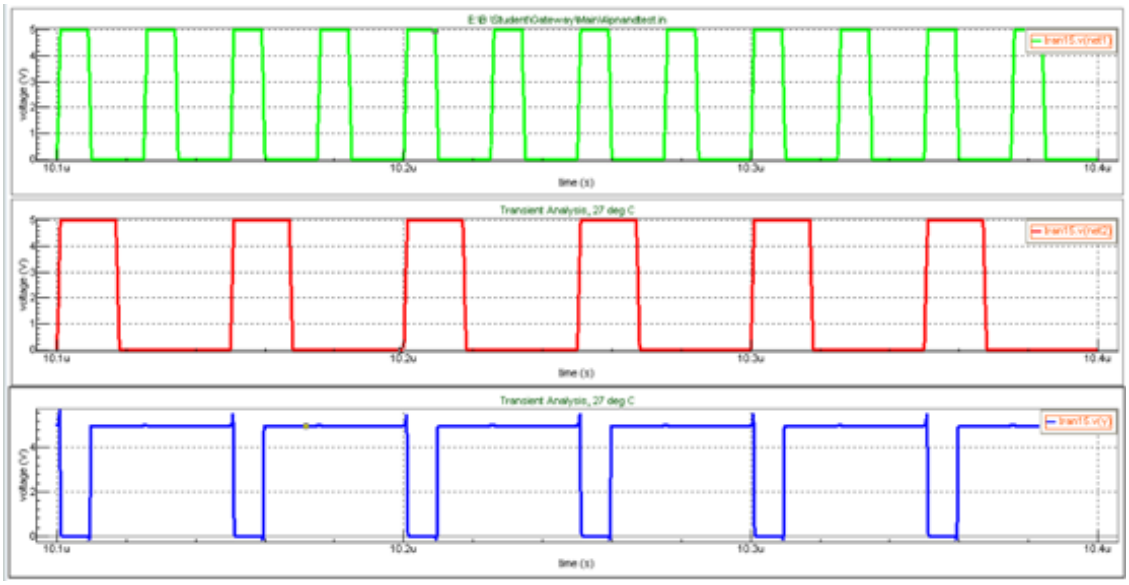

Figure 3.3: SmartSpice example waveform

3.4 PARAMETER SPECIFICATION

Before designing the circuits, parameter of the NMOS and PMOS must be specifying. Value of PMOS must be double of the NMOS size following the normal ratio so the speed for both transistors is the same. Ratio for static CMOS is 2/1 for dynamic circuits [14].

Table II All NMOS and PMOS parameter

	All PMOS	*All NMOS*
Width	6µm	3µm
Length	0.18µm	0.18µm

3.5 SILVACO EDA GATEWAY SOFTWARE

After the parameters of the transistor have been set, the circuits of comparator are design. SILVACO EDA Gateway tools are used to design the circuits. Equality comparator and zero/one comparator are constructed using SILVACO EDA Gateway. Figure 3.4 and figure 3.5 the proposed 4 input pair equality comparator and zero/one comparator. These two comparators then combined to create a 64-bit dynamic

comparator. The proposed circuit of an 8-bit zero/one comparator is shown in Figure 3.5. When the CLK is low, Node 0 is precharged to VDD. When REF is set high, D0, D1, D2, D3, D4, D5, D6 and D7 also high, then M15, M16, M17, M18, M19, M20, M21, M22, M23 and M24 are on while M2, M3, M4, M5, M6, M7, M8, M9 and M10 are all off. So, Node 0 kept in high and there is no current path exists during the period.

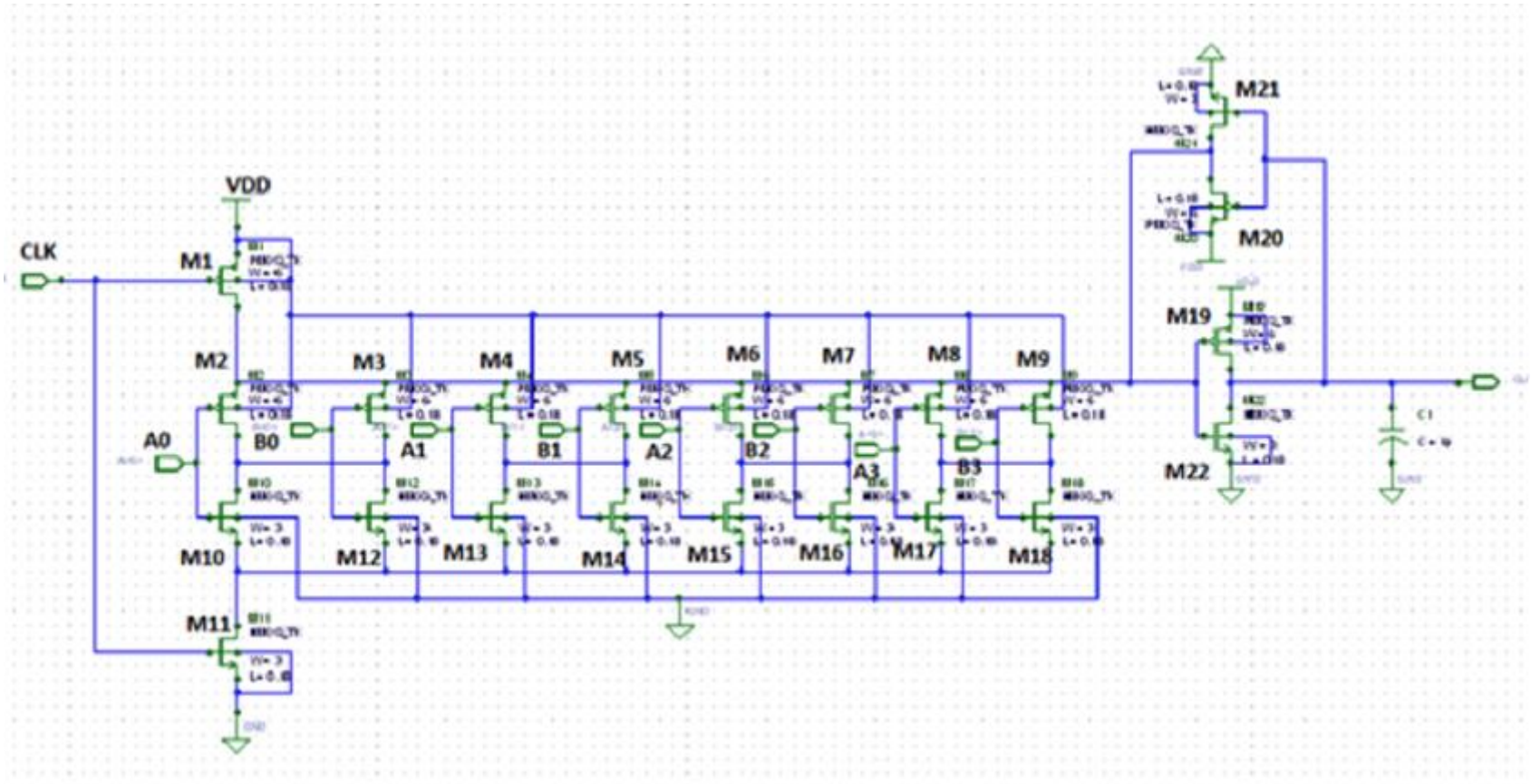

Figure 3.4: Proposed 4 input pair equality comparator

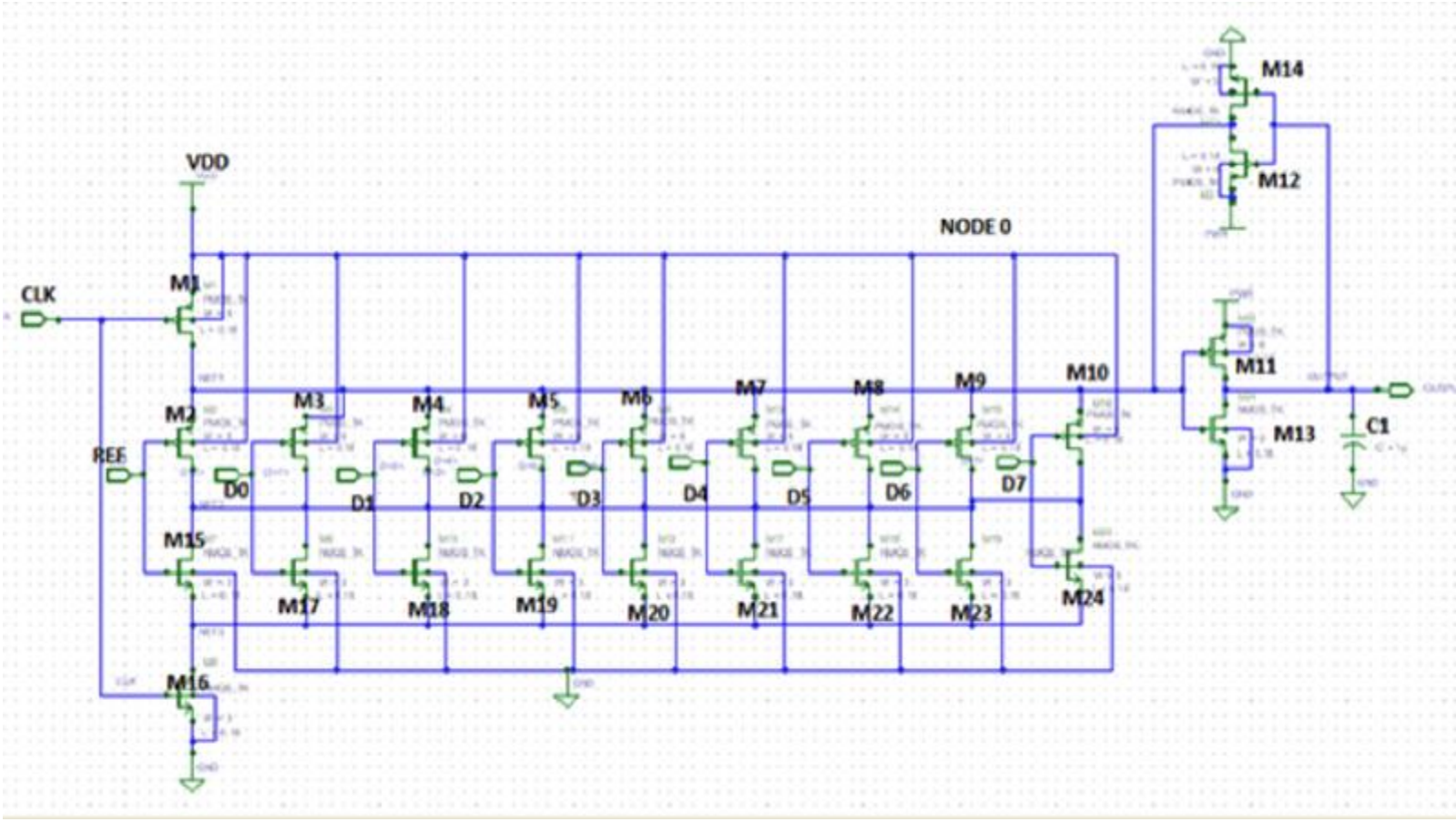

Figure 3.5: Proposed 8-bit zero/one comparator circuit

3.6 COMPARATOR BLOCK DIAGRAM

Figure 3.6 shows the block diagram of the design comparator. Firstly, the 4-bit input pair equality comparator is connected such as in figure 3.7 to create an 8-bit equality comparator. Output of the equality comparator is connected to the OR gate so the output value is limited to 1 or 0 because of the characteristic of the OR gate. Then the 8-bit equality comparator is connected to become one 64-bit input equality comparator. The output of the equality comparator then connected to the 8-bit zero/one comparator. The zero.one comparator produces output zero or one if all the input are same. This topology connected together to create one 64-bit dynamic comparator.

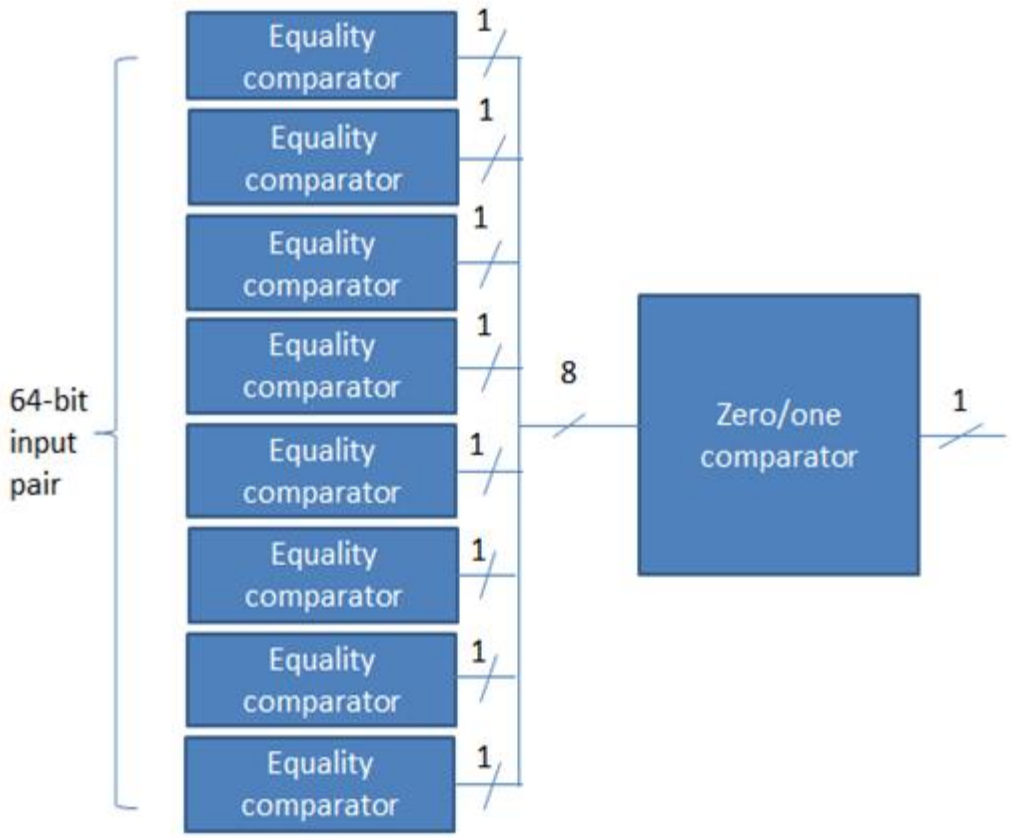

Figure 3.6: Block diagram of comparator

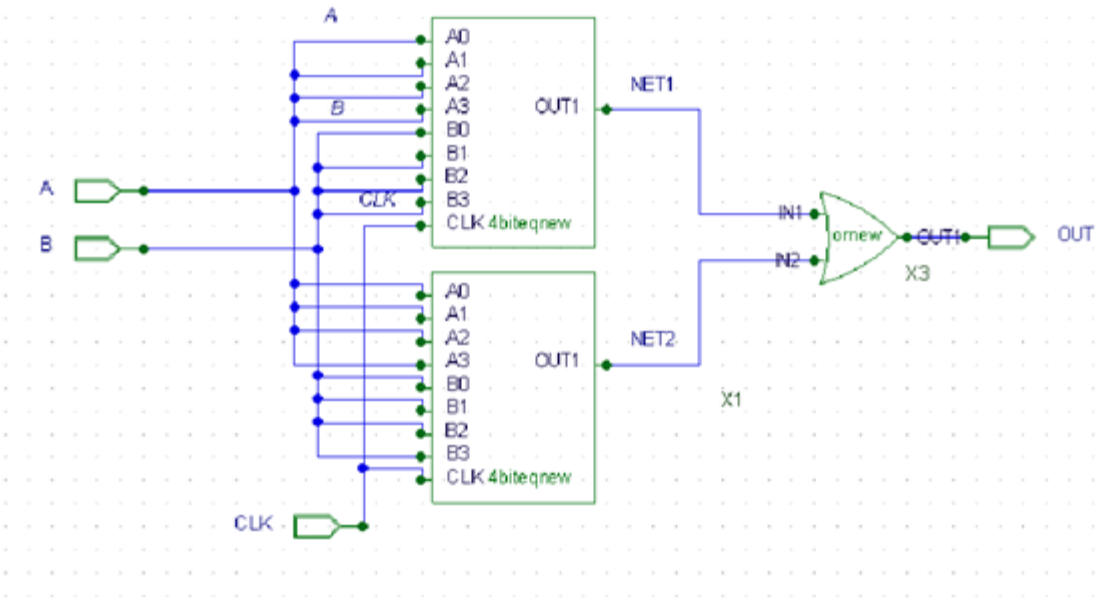

Figure 3.7: 8 bit equality comparator

3.7 INVERTER

Static CMOS inverter consists of one NMOS and one PMOS that connected in series. Figure 3.8 shows the static CMOS inverter symbol and figure 3.9 shows the static CMOS inverter circuit. Static CMOS inverters are connected on the output of both equality and zero/one comparator as shown in figure before.

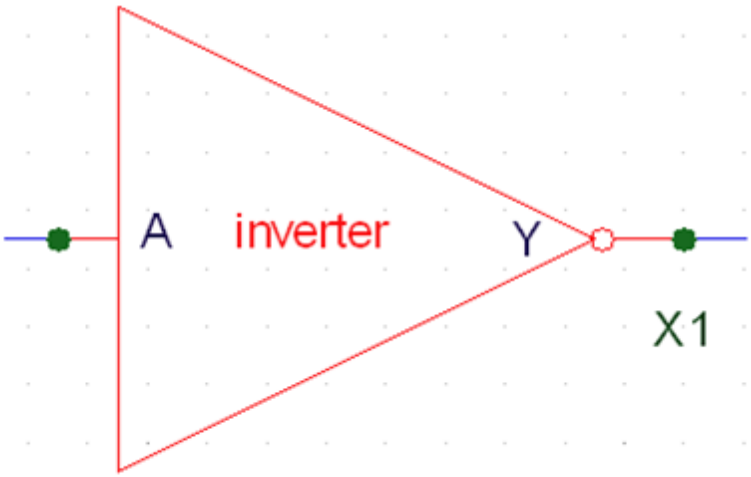

Figure 3.8: Inverter symbol

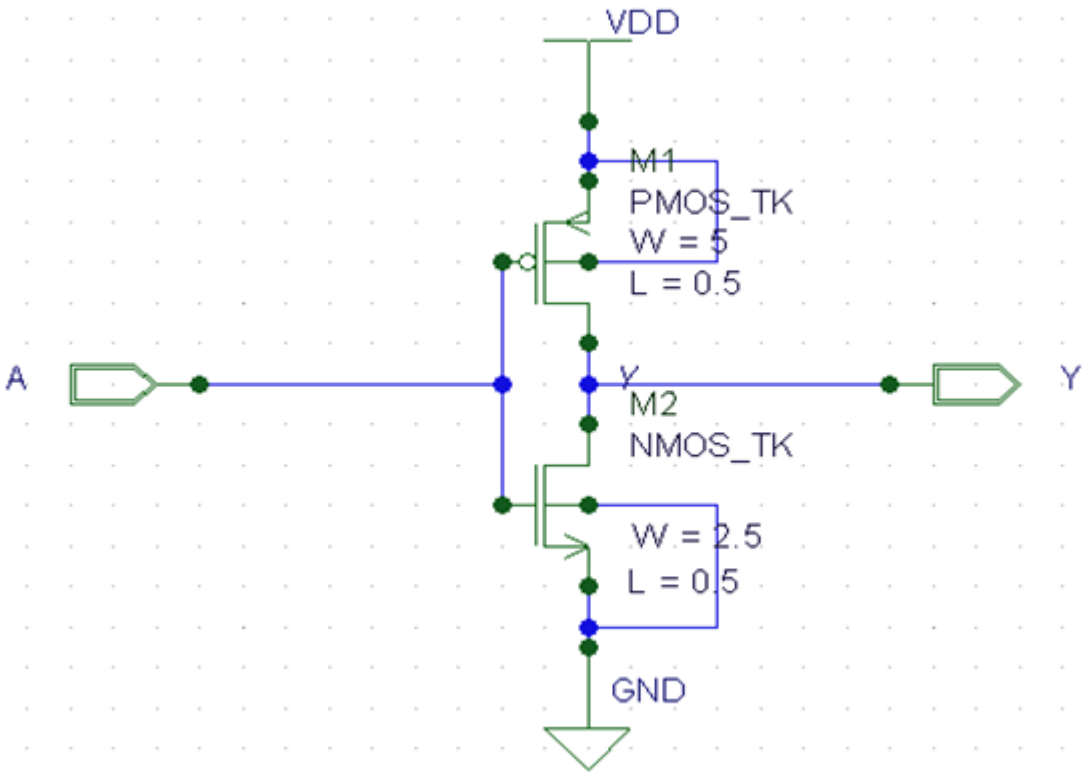

Figure 3.9: Static CMOS inverter

3.8 TESTBENCH

A test bench or testing workbench is a virtual environment used to verify the correctness or soundness of a design or model, for example, a software product Testbench are important step in the design. This step is important to check whether the circuit design in this project can produce output when the circuit is simulated. Figure 3.10 shows the testbench circuit used to simulate or use for transient analysis to get the results.

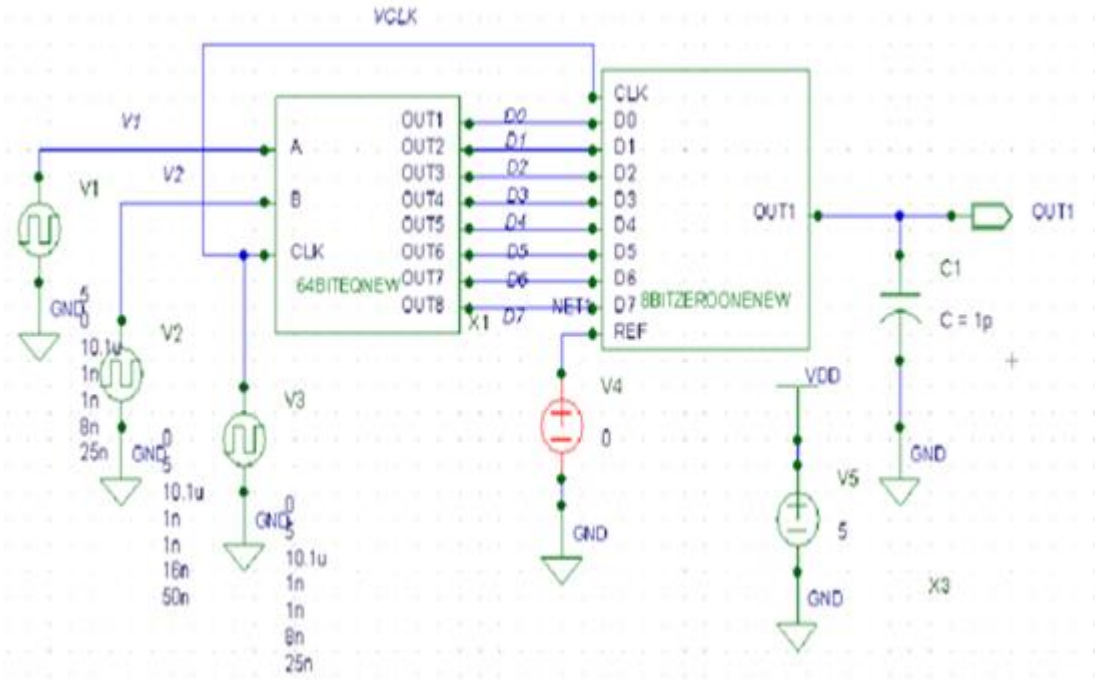

Figure 3.10: Testbench circuit

Figure 3.10 shows the final topology of dynamic comparator. It consists of proposed equality comparator and proposed zero/one comparator circuits. Vpulse is use for the input of CLK, A and B. Values of A and B varies to give different waveform input for the comparator circuits. This allows the output waveform to show different output when input is 1 or 0. Capacitor use at the end of the output during testbench to rectify or smooth the DC output waveforms. 5V voltage supply was used for both technologies but the CMOS technology is different. This project wants to determine of the effects when different CMOS technology used in a comparator without disturbing the value of voltage supply.

CHAPTER 4

RESULT AND DISCUSSION

4.1 INTRODUCTION

This chapter will be discussing the result of the project. Simulation using transient analysis used to obtain the results for the parameter chosen. The results that obtained are the propagation delay of the comparator using 0.18µm technology and 0.5µm technology and the power dissipation of the comparators. In this chapter also show the effect of waveform using different CMOS technology.

4.2 SIMULATION WAVEFORM

Simulation for transient analysis is done using 0.18µm CMOS technology. 5V voltage supply is used and clock period used is 8ns for transient analysis. This design used to determine the power and delay/speed. Simulation results of the comparator are shows in Figure 4.1, Figure 4.2 and Figure 4.3. The width of the transistor used is as in the Table II. This simulation result is compared to the previous work by [1]

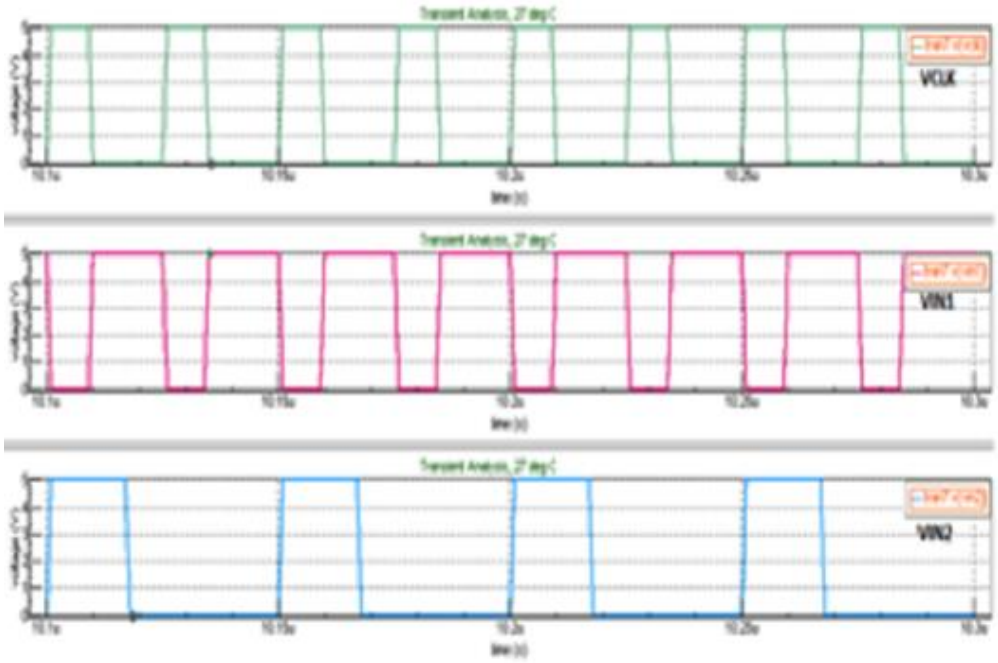

Figure 4.1: Input waveform

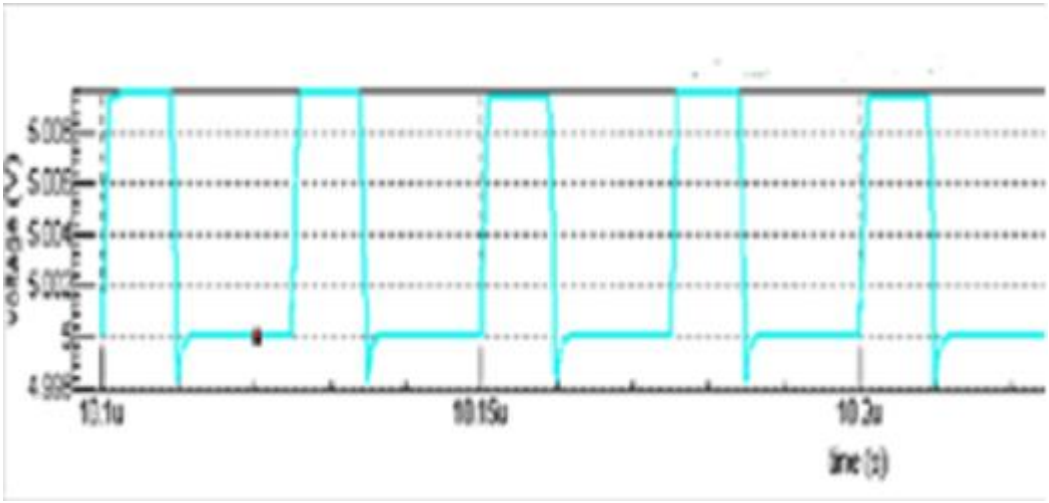

Figure 4.2: Output waveform for 0.18µm technology

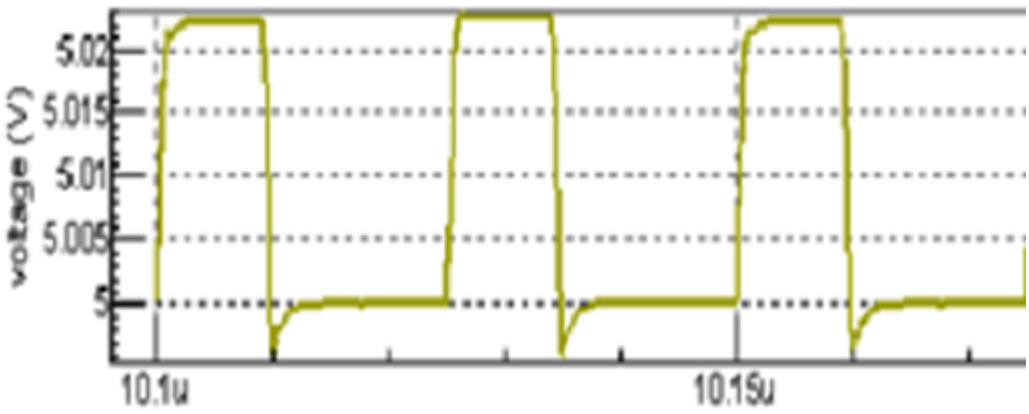

Figure 4.3: Output waveform for 0.5µm technology

4.3 EFFECT OF PARAMETER CHOSEN

0.18µm technology use in this project, which is smaller length than technology, used in the previous work by, so length of PMOS and NMOS for this project is 0.18µm. Simulation in Figure 4.4 shows the different in the output when different technology is chosen.

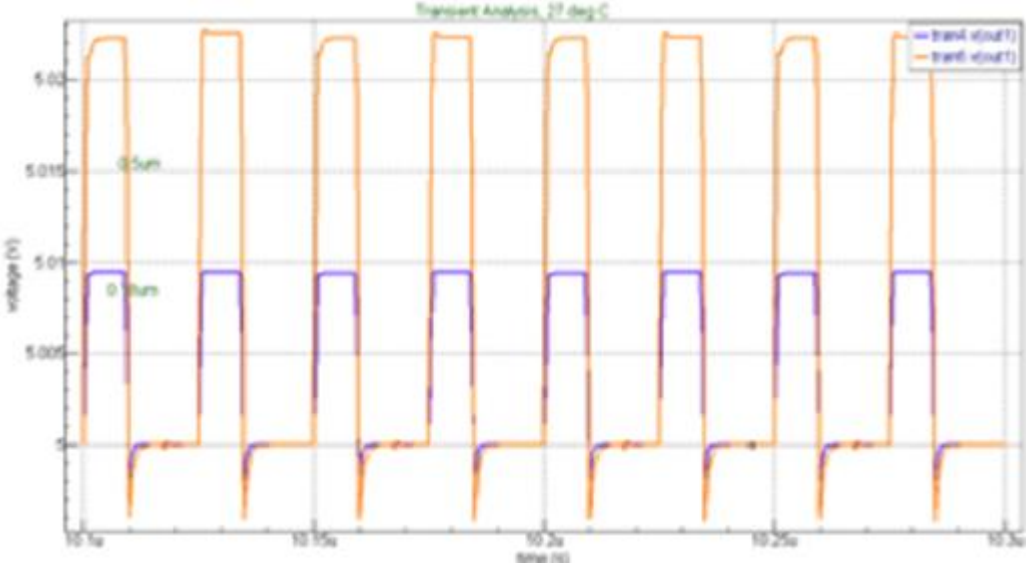

Figure 4.4: Output waveform with different length

4.4 PROPAGATION DELAY

Propagation delay and settling time are the most important parameters to determine the speed of the comparator designed. Propagation delay is the amount of time that it takes for a change in the input signal to produce a change in the output signal. Delay time is measured at 50% transition of the point. The propagation delay is determined using two basic time intervals, which is tPLH and tPHL. tPLH is the delay time measured when output is changing from logic 0 to logic 1 and tPHL is from logic 1 to 0[15]. Propagation delay is the sum of tPLH and tPHL and then divides by 2. In this project, delay is measured using the SILVACO tools. Different technology produces different delay. The smallest delay, the fastest the speed. Figure 4.5 and 4.6 show the different delays when using different CMOS technology.

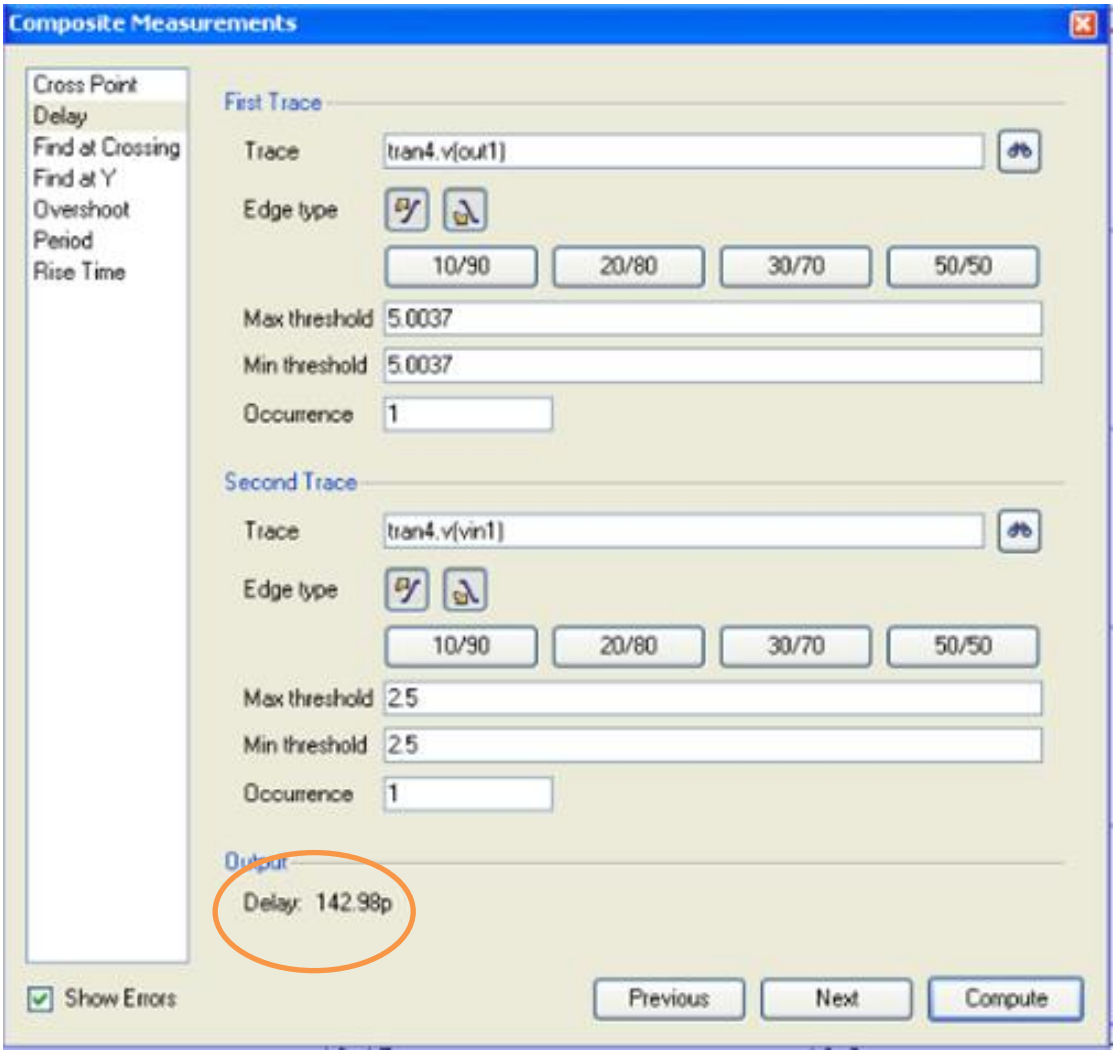

Figure 4.5 Delay of 0.18µm technology

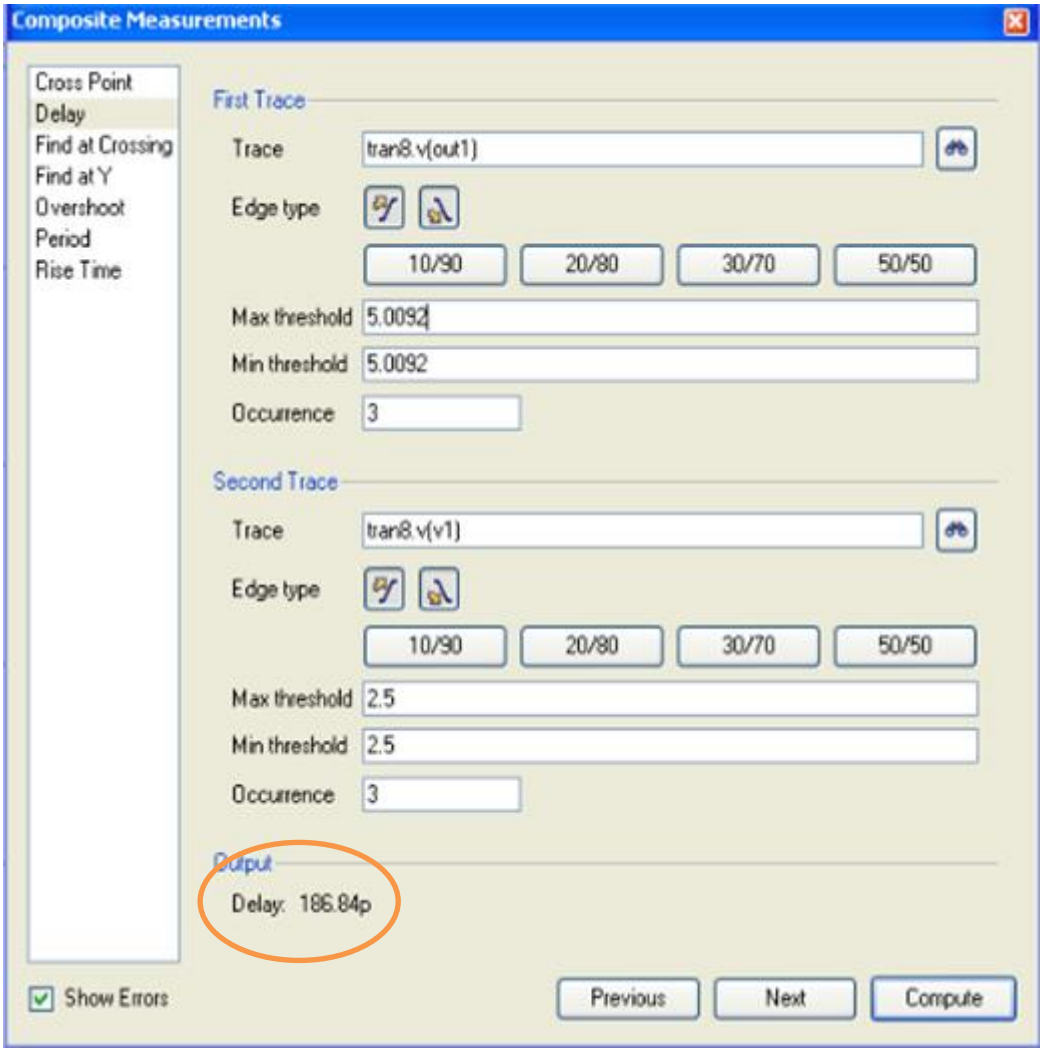

Figure 4.6: Delay of 0.5µm technology

Simulation shows that the delay of 0.18µm technology (142.98p) is smaller than the 0.5µm technology (186.84p). This shows that the 0.18µm technology is faster than 0.5µm technology. The speed of the comparator has increase 93% than the previous technology [1] that using HSPICE.

4.5 POWER DISSIPATION

Next important parameter is the power dissipation of the comparator [5]. Power dissipation need to be reduced to reduce noise and cost. Power dissipation is power that is transform into a heat and then radiated away from the devices. Power dissipation can be determined by multiply the current, IDD with the supply power, VDD as shown in Eq. (1)[16].

$$P = V_{DD} \times I_{DD} \quad (1)$$

Figure 4.7 shows the total current of the 0. 5µm technology and Figure 4.8 shows the total current of the present work using 0.18µm technology. From Eq. (1) [1], the power dissipation for 0.5µm technology is 3.67nW and for the current work is 3.81nW. The power dissipation for 0.18µm technology is higher than 0.5µm technology. Although the power is high, the power range is still 3.5nW to 4.0nW. So, this comparator is still power efficient although it using smaller technology and same power supply value from the previous technology [1]. Theoretically, when the speed increases, the power dissipation also increases.

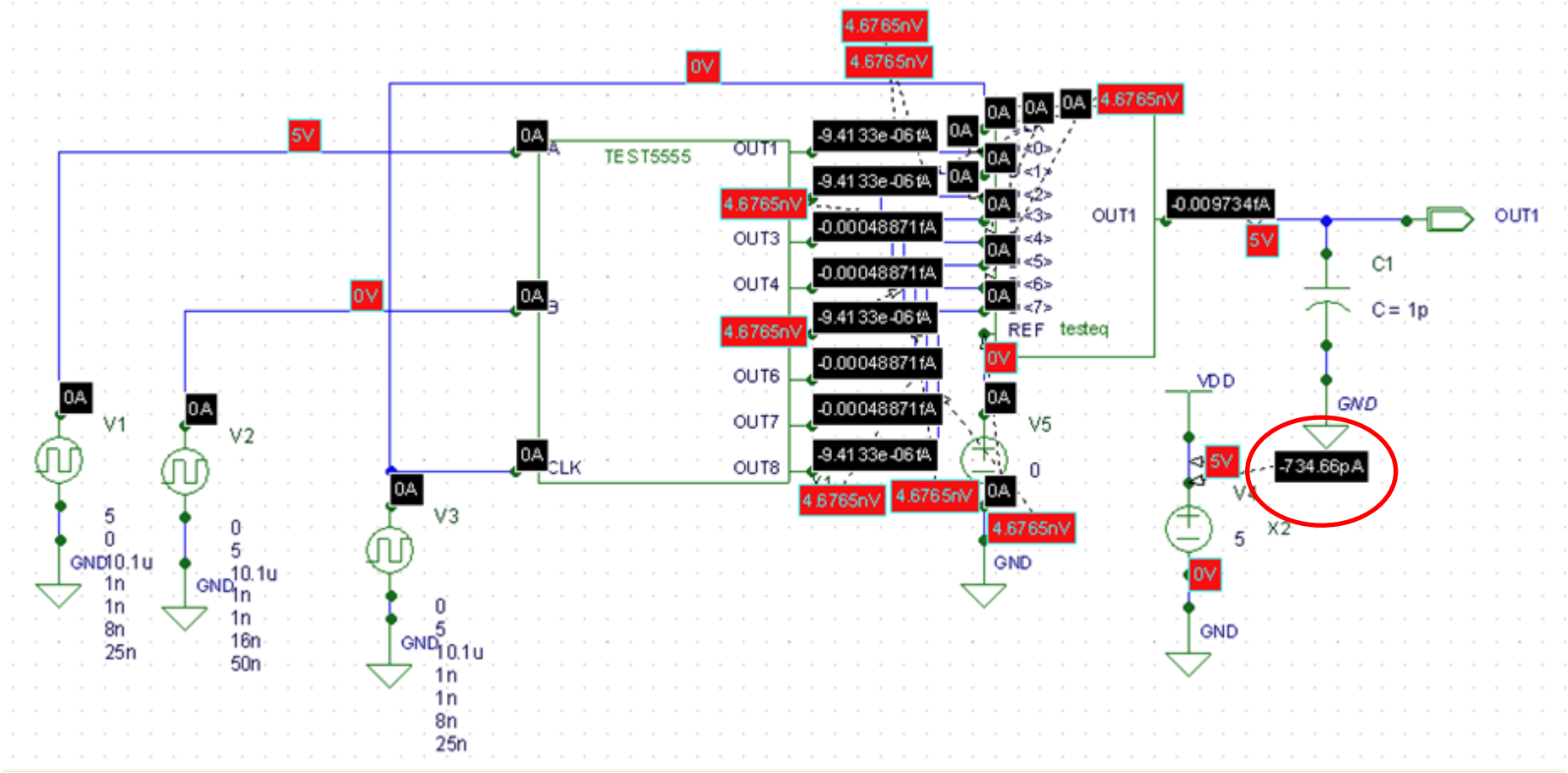

Figure 4.7: Total current of the 0. 5µm technology

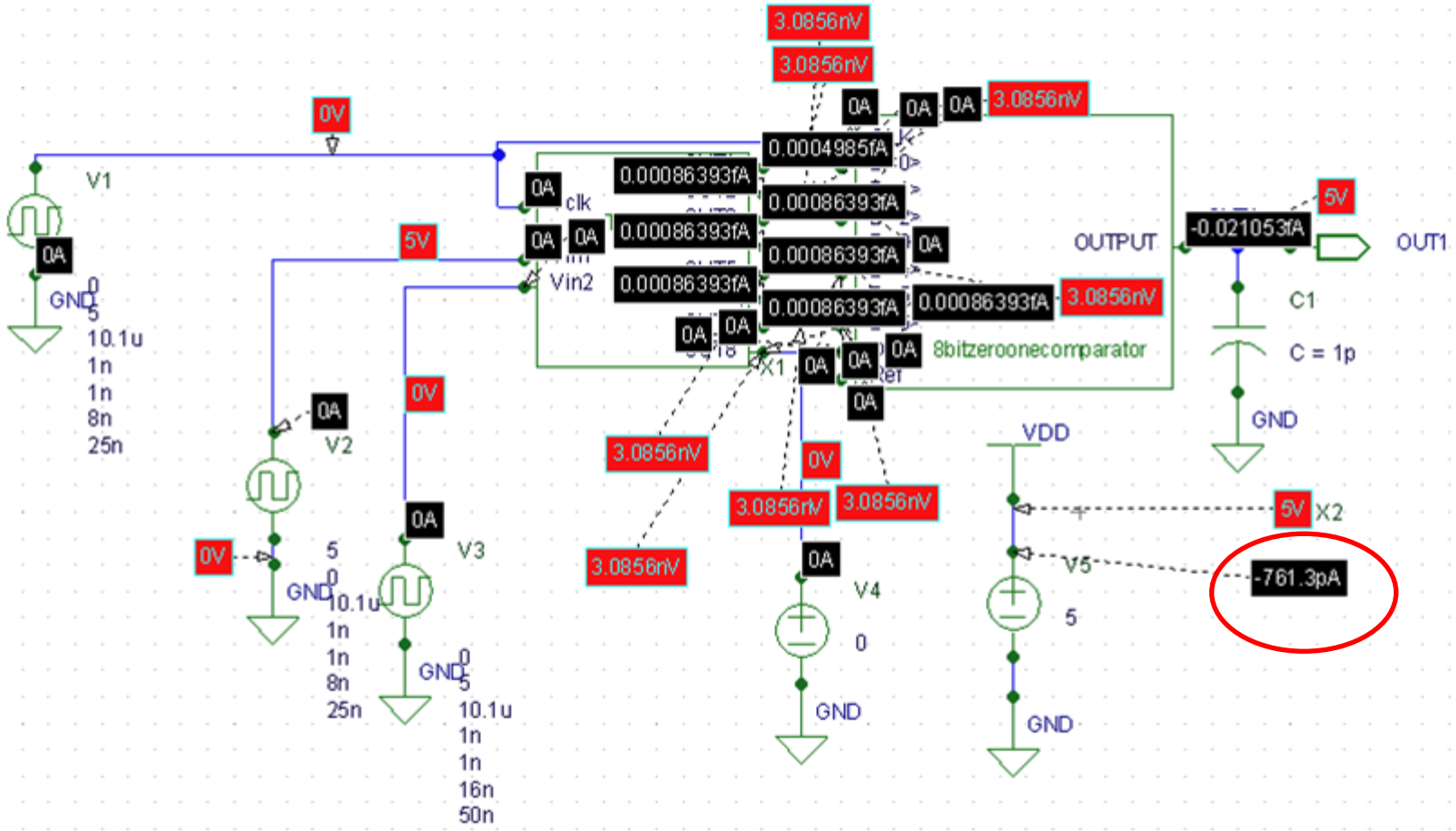

Figure 4.8: Total current of 0.18µm technology

4.6 AVERAGE POWER DYNAMIC

Average power is the energy converted per unit of time. The energy consumed over some interval time, T is the integral of the instantaneous power [5].

$$E = \int_0^T I_{DD}(t)V_{DD}dt \qquad (2)$$

The average dynamic power dissipation over this interval is shows in Eq. (3) [5]

$$P_{avg} = \frac{E}{T} = \frac{1}{T}\int_0^T I_{DD}(t)V_{DD}\,dt \qquad (3)$$

The integral finds the average current delivered by VDD. Using the SEedit, average dynamic power can be measured automatically. Results of the average dynamic power dissipation are shown in Figure 4.9 and 4.10.

Index	tran6.p[v4][w]
1	3.67328e-009

Figure 4.9: Average power for 0.5µm technology

Index	tran4.p[v5][w]
1	3.80648e-009

Figure 4.10: Average power for 0.18µm technology

4.7 COMPARISON WITH PREVIOUS TECHNOLOGY

After all the results has been obtained, the results than compared with the previous technology [1]. The delay result is compared between the 0.18µm CMOS technology for SILVACO EDA with the 0.5µm technology for the HSPICE. Figure 4.11 shows the delay for the HSPICE software. The 64-bit comparator delay for 0.5µm technology using HSPICE is 2.126 for clock to output and 2.120 for input to output.

Table III shows the simulation results for the proposed comparator using SILVACO EDA. For 0.5µm technology, the delay is 186.84ps and the power dissipation is 3.7183nW. For the 0.18µm technology, the delay result is 142.98ps smaller than the 0.5µm technology. The power dissipation for 0.18µm technology is 3.8065nW, bigger than 0.5µm technology.

TABLE VI The delays of the proposed 64-bit comparator

I/O path	Delay (ns)
clk → output	2.126
input → output	2.120

Figure 4.11: HSPICE delay output

Table III SILVACO EDA results

TECHNOLOGY	DELAY	POWER
0.5µm	186.84ps	3.7183nW
0.18µm	142.98ps	3.8065nW

CHAPTER 5

CONCLUSION AND FUTURE DEVELOPMENT

5.1 CONCLUSION

The Power Efficient 64-bit Dynamic Comparator using 0.18µm technology is successfully designed. The speed and power of the design successfully obtained and compared with the previous technology [1]. The delay of the comparator successfully reduced but the power dissipation is increased considering the comparator using same voltage value as previous technology [1]. The delay has been decreased about 93.27 % but the power increased 2.32 %. Comparator still considers as power efficient because the power does not increase much from 3.7183nW to 3.8065nW. From the theory, if the speed increases, the power dissipation also increases. This can be shown on the CPU. The increases of the speed make the CPU heats faster. The width and length are adjusted to minimize the delay and power for the comparator. Value width is different for different technology and the value must satisfy the ratio of static CMOS in dynamic logic. Table IV shows the conclusion for the technology compared.

TABLE IV Comparison of technology

	0.5µm (SILVACO)	**0.18µm (SILVACO)**	**0.5µm (HSPICE)**
Length	0.5µm	0.18µm	0.5µm
Wp/Wn	10/5	6/3	-
Voltage Supply	5v	5v	5v
Delay	186.84ps	142.98ps	2.126ns
Power	3.7183nW	3.8065nW	-

5.2 FUTURE DEVELOPMENT

Through research and development done to accomplish the project, recommendations are proposed to improve the performance of the design.

It is recommended to apply 45nm technology in this power efficient 64-bit dynamic comparator to obtain lower power and higher speed. Lower power supply also can be used to obtain the lower power dissipation for this comparator.

This can be achieved by using appropriate software that can support this technology without any problem. To use SILVACO EDA tools, the scale of NMOS and PMOS need to be change to make sure there is no problems occur regarding of the software's limitation

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