CACHE COHERENCE PROTOCOLS IN MULTI-PROCESSOR

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ABSTARCT

The data coherence in the cache systems in multi-processors is expected to be more precise and reliable. There is no doubt that many approach has been taken in order to achieve that purpose. This thesis describes one of the approaches which is the cache coherence protocols in multiprocessor. A cache coherence protocol ensures the data consistency of the system. Typical modern microprocessors are currently built with multicore architecture that will involve data transfers between from one cache to another. By applying cache coherence protocols to each of the caches, the coherency problem can be solved. With this resolution, simulations of the applied cache coherence protocols can be each presented to walk-through the coherency processes in multi-processor. This simulation is developed based on Verilog Coding and implemented using Xilinx Software. Using the same software, test benches were constructed to verify the functionality for each of the protocols. The cache coherence protocols consist of read operations and writes operations of the cache which will be elaborated and discussed in this thesis. Based on the result, it can be seen the flow of the data transfers and the improvements of each of the protocols has brought on improving the cache system by designing a simple system that consist of a cache, a coherence protocol, and a memory. This thesis is hoped to be a help in understanding of the data transfers and coherency in cache systems and help to motivate in enhancing the current system for better performance of multi-processor. It is recommended that this design to be implemented in real life to validate the system for further development of this project.

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CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

As Moore's Law [2] predicts, hardware is becoming progressively smaller and execution times quicker. The current hardware world is dominated by the multi-cores or many-cores [3]. As the trend shifts from single-core to multi-core processors for tuning up the performance, system architectures have several alternatives on one of the most important system resources-the cache. In multiprocessor architectures, caching plays a very important role and it is actually the key to the performance of the processor. In all-cached architectures, any information is transferred into the primary cache first before being used. Unfortunately, the presence of writable shared information in caches introduces the problem of Cache Coherence. The cache coherence problem arises from the possibility that more than one cache of the system may maintain a copy of the same memory block. Cache coherence is the discipline that ensures that changes in the values of shared operands are propagated throughout the system in a timely fashion. Therefore, some basic protocols are adapted in order to eliminate the problem of cache coherency in the memory system such as Snooping Protocol and Directory Protocol. Accordingly, different multiprocessors based systems implement different cache coherence protocols that have given birth to different protocol verification logics. This thesis studies the cache coherence mechanism in multiprocessor environment by designing a simple cache and memory to serve as a platform to implement the cache coherent protocols which also focuses only in write invalidate type of Snooping Protocols such as MSI, MESI, and MOESI. With the simulations obtained, the changes between states of each of the coherence protocols can be witnessed and analyzed for educational purpose and to further the development of the invented protocols