INVESTIGATION OF ELECTRICAL CHARACTERISTICS OF FULLY-DEPLETED SOI DEVICE

This report is presented in partial fulfillment for the award of the
Bachelor of Electrical Engineering (Hons)
UNIVERSITI TEKNOLOGI MARA
MALAYSIA

ZULHELMI BIN ABU HASAN
FACULTY OF ELECTRICAL ENGINEERING
UNIVERSITI TEKNOLOGI MARA
40450 SHAH ALAM SELANGOR
MALAYSIA

ACKNOWLEDGEMENT

In the name of Allah, Most Merciful, Most Compassionate. It is by God's willing, I was able to complete this project within the time given. This project would not have been possible without the support of many people.

Firstly, I would like to take this opportunity to thank my supervisor, Miss Yusnira Husaini for his guidance, patience and support for me throughout the period of time in doing this project. Without her guide and encouragement the project may not achieve its goal.

Besides, I would like to thanks those who have indirectly contributed their opinion and effort to realize this project successfully especially to all my family who support behind me and also not forget to mention to all of my friends who give strength and cooperation during my thesis in order to finish this project successfully.

Lastly I would like to thank all staff and lecturers of Faculty of Electrical Engineering, Universiti Teknologi Mara Malaysia for their help and support. May God bless them and reward them for their generosity.

ABSTRACT

This project is to investigate and to simulate the electrical characteristics of fully-depleted SOI (silicon-on-insulator) and bulk-Si n-MOSFET devices in order to compare their electrical characteristics. The comparisons were focused on three main electrical characteristics that are leakage current, threshold voltage and subthreshold voltage. Two specific channel lengths of the device that had been concentrated are 0.5 and 0.35 micron. All the process and device simulations were done using SILVACO TCAD software. The device structures were constructed using Silvaco-Athena and Atlas-Syntax while the electrical characteristics were examined and simulated using Silvaco-Atlas. Results were analyzed and presented to show that the electrical characteristics of fully-depleted SOI devices are better than bulk-Si devices. It has also shown that the fully-depleted SOI device is superior in the submicron region.

TABLE OF CONTENT

CHAPTER	LIST OF TITLE	PAGE
	DECLARATION	III
	DEDICATION	IV
	ACKNOWLEDGEMENT	V
	ABSTRACT	VI
	TABLE OF CONTENTS	VII
	LIST OF FIGURES	XI
	LIST OF TABLE	XIII
	LIST OF ABBREVIATIONS	XIV
	SYMBOLS	XVI
1	**INTRODUCTION**	1
	1.1 BACKGROUND OF STUDY	1
	1.2 PROBLEM STATEMENT	3
	1.3 OBJECTIVES	3
	1.4 SCOPE OF THE PROJECT	3
	1.5 ORGANIZATION OF THE REPORT	4
	1.6 SUMMARY	5
2	**LITERATURE REVIEW**	6
	2.1 INTRODUCTION	6
	2.2 SILICON ON INSULATOR (SOI)	6
	2.2.1 The Advantages of SOI	7
	2.2.2 History of Development of SOI Technology	9
	2.2.3 Fabrication of SOI Wafers	10
	2.2.3.1 Hetero-Epitaxial Technique	11
	2.2.3.2 Homo-Epitaxial Technique	11
	2.2.3.3 Recrystallization Technique	11

CHAPTER 1

INTRODUCTION

This project uses Silvaco Athena, Atlas Syntax and Atlas as a primary fabrication process and simulation tool. First part of the report will elaborate more on the background of study. Second part will describe on problem statement that related to the study. This chapter also mentions on the objective, scope of the project and last part of the report will briefly describe the organization of the report.

1.1 BACKGROUND OF STUDY

Silicon technologies have progressed rapidly year by year. The main issue has been concentrated on much the silicon devices can be scaled down and to be able for production [1]. The smaller MOSFET very interesting nowadays because smaller MOSFET allow more current to pass and it also has smaller gate, thus lower capacitance. It can result the increasing speed of the device and lower power consumption. Besides, another reason for scaled down MOSFET, which is smaller MOSFET can be packed more densely, resulting smaller chips and chips with more computing power in an area.

According to Sir Gordon Moore prediction, which popular by the name of Moore's Law in year 1965, he predicted that transistors would continue to shrink, allowing double transistor density in single IC every 18-24 months and double performance every 18-24 months. Due to the increasing numbers of transistor in a single chip, each transistor size needs to decrease geometrically. As the size of