MULTI-SIZED OUTPUT CACHE CONTROLLERS

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Bachelor of Engineering (Hons.) Electronic
UNIVERSITI TEKNOLOGI MARA (UiTM)
SHAH ALAM, MALAYSIA

MOHD NAQIB BIN JOHARI
FACULTY OF ELECTRICAL ENGINEERING
UNIVERSITI TEKNOLOGI MARA
40450 SHAH ALAM
SELANGOR DARUL EHSAN

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ABSTRACT

This thesis describes the design of a Multi-sized Output Cache Controller that will handle 2Kbyte 16 ways with 4 word block size cache. A cache controller is a device that used to sequences the read and write of the cache storage array [1]. Most of modern microprocessor is designed with multiple core architecture that will lead to massive traffic of cache data transfer. By taking the advantage of using temporal locality and spatial locality to the cache, the problem can be solved. With this solution, a controller that capable to handle huge amount of way and block size need to be designed. It also should have the capability overcome the cache coherence. This design will be implemented using Xilinx software. It was developed base on Verilog coding. Using the same software, a test bench was constructed to test the functionality of the controller. This cache controller consists of four stages, from request to read data. It had the capability to read and write to different agent on various output data size from 1byte till 16 byte.

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CHAPTER 1

INTRODUCTION

1.1 BACKGROUND OF STUDY

Throughout the last decades, the technology of digital electronic have become more advance. As the times goes on, this advancement have made the computer and other electronic hardware such as mobile phone, PDA and many electronics gadget become smaller, faster and cheaper to produce. Most of these devices are using microprocessor as their brain to control their operation. Nowadays, making a faster microprocessor is the main concern. One of the important components inside the microprocessor is the cache controller. As the microprocessor speed vastly increases, designing a much faster cache become very important [2][3].

One of the ways to improve the cache controller is by executing a pipelined cache controller [4]. However, this solution will increase the complexity of the circuit. Multicore architecture was introduced to increase the processing speed and had been widely use over the world due to its high performance [6]. As the multicore system allow to process multiple applications simultaneously, the cache controller was introduced to overcome the problem existed during all the cores sharing cache memory on a single dye [6]. However, the cache controller needs to be fast enough to deals with this massive data transfer between cache, memory and the processor.