MULTIPLIER INTEGRATED CIRCUIT DESIGN FOR DIGITAL NEURON USING 0.13µm TECHNOLOGY

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ABSTRACT

Neural Network is artificial intelligence system that consists of multiplication and addition process. The Neuron Network is made from lot of multiplier and adder. The objective is to design an adder and multiplier integrated circuit for neuron architecture. Comparison is done between multiplier architectures, array and booth to neuron performance. The adder that is use in the design is ripple carry adder. For array multiplier, two structure of multiplier that was built 10x5 bit multiplier and 8x8bit multiplier. For Booth multiplier the multiplier is build using verilog code in Quartus software. After that ring structure of neuron was selected to be investigated the effect of the multiplier. The performances are evaluated in terms of number of bit, power, fan-out, and timing analysis. For the data, it was found that Booth multipliers are giving the less time delay, less power, less fan-out and also less logic element. Result shows that ripple carry adder and booth multiplier have almost same power, 196.9mW. For other performances booth is give less value, which is fan-out 467, logic element 103 and timing 19.984ns. For over all study show that booth multiplier performance is better than array multiplier.

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CHAPTER 1

INTRODUCTION

1.1 Introduction

This project focuses on the multiplier integrated circuit design for digital neuron using 0.13µm technology. The multiplier and neuron are designed using custom design approach. The multiplier design for this project is covering array and Booth architecture.

1.2 Project Background

Neural network has been used in many applications in science and engineering. The most common architecture consists of multiplier perceptrons trained the back error-propagation algorithm (MLP-BP). Neural network contains lot of neuron that be arranged in hierarchical. Multiplier is the base component to build a neuron. Although multiplier has many type base on the design. It make the multiplier different have different performance. In this project, investigate the effect of different multiplier to the performance of neuron in terms of area, time delay and power. There are two type of multiplier that is investigate, one is array multiplier and another one is booth multiplier. The multiplier will be use in ring neuron structure.

This project is to design a multiplier in integrated circuit for neuron using 0.13µm technology. The two type multiplier will be investigating in term of power, time delay, fan-out, area and logic elements. The output data from the multiplier will