DESIGNING CLOCK GENERATOR AND BCD COUNTER FOR A FREQUENCY COUNTER USING VHDL

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ABSTRACT

This paper presents a development of a frequency counter using VHDL under Xilinx environment. This frequency counter is based on the premise of counting the incoming known frequency's rising edge for digital signal as a predetermined fixed amount of time, or GATE. The circuit is partitioned in two sequences individual circuit namely as Clock Generator and BCD Counter. The sub circuits for clock generator are Oscillator 4 (OSC4) and counters according to the chosen frequency generated. The circuit for BCD Counter is a main circuit. There are three types of modelling used as an existing method such as behavioural, structural and data flow. Other modelling technique that is also considered is the state machine as an additional method which is coded using VHDL where the results are observable in form of timing diagrams.

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CHAPTER 1

INTRODUCTION

1.1 Introduction

The main purpose of this project is to design two major circuits namely Clock Generator and BCD Counter. The Clock Generator circuit comprises of sub circuits, the mode counter and the oscillator (in the oscillator, fix frequencies are chosen to produce desired frequencies). As for the BCD counter, the basic element includes the block for conversion for BCD to 7-segment in the frequency counter. All the components required were coded using VHDL programming under Xilinx environment.

1.1.1 Counter at Rising Edge

One potential use for counters is to measure the period, or the length of time between successive rising edges, of an incoming signal. A known frequency, usually an internal clock, is used as a reference. The counter starts counting at a rising edge, which is user-configurable, and stops counting at its successive edge [1]. As in Figure 1.1 the pulse period is the number of counts between rising edges divided by the number of counts expected in one second (frequency of the known clock), that is, period = counts / frequency [1] as in Figure 1.2 assume period T = 1.

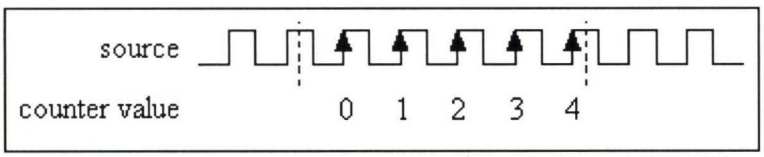

Figure 1.1: Frequency rising edge