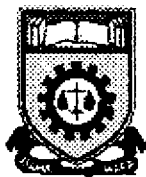


**THE ANALYSIS OF A SECOND ORDER BANDPASS FILTER OF A LOW
NOISE CMOS INSTRUMENTATION AMPLIFIER USING MENTOR
GRAPHICS**

This thesis is ~~presented~~ presented in partial fulfillment for the award of the
Bachelor in Electrical Engineering (Hons.) of
INSTITUT TEKNOLOGI MARA.



HANIZA BT BURHAN
Faculty of Electrical Engineering
Institut Teknologi MARA
40450 Shah Alam
Malaysia
NOVEMBER 1998

Abstract

This thesis presents a report on my project titled "The Analysis of A Bandpass Filter of A Low Noise CMOS Instrumentation Amplifier Using Mentor Graphics". This project was taken from the IEEE Journal of Solid-State Circuits, Vol. 32, No 7, July 1997[2] where in my experiment; the bandpass filter is a part of the instrumentation amplifier mentioned above. The circuit has its requirement that must be observed. The circuit is first drawn using Mentor Graphics (Design Architecture) where all the rules and regulation for the electrical codes are obeyed. The AccuSim, one of the modules in Mentor Graphics, is used to simulate the circuit. The result is a bandpass filter with a response of a resonant frequency at 5.0873kHz a voltage gain of 25.492 (27.794dB) and a Q-factor of 3.793.

Acknowledgement

In the name of ALLAH the Most Gracious, Most Merciful and HIM alone is worth all praises.

I would like to express my gratitude to my Project Supervisor, Pn Azilah Saparon, for her guidance, patience, encouragement and cooperation in supervising me through out accomplishing this project. My gratitude also goes to the Computer Lab. Assistants, for their cooperation.

**THE ANALYSIS OF A BANDPASS FILTER OF A LOW NOISE CMOS
INSTRUMENTATION AMPLIFIER USING MENTOR GRAPHICS**

<u>Content</u>	<u>Page No.</u>
Abstract	i
Acknowledgement	ii
Figures and Tables	v
INTRODUCTION	1
PROBLEM STATEMENT	3
2.1 Objectives	3
THE COMPONENT	8
3.1 MOSFET	8
3.2 MOS Transistors	8
3.3 The Enhancement type MOSFET (EMOSFET)	11
3.4 MOS Capacitance	15
3.5 Junction Capacitance	16
THE CIRCUIT	17
4.1 Filter	17
4.2 The Filters Topologies	17
4.3 The Gm-C Technique	19
4.4 The Circuit Implementation	22
4.5 A Linear CMOS Transconductor	23
4.6 Practical Limitation Of Gm (OTA) based integrator	24
4.7 MOS Capacitors	25
4.8 Linear Filtering Concepts and Definitions	27
THE SOFTWARE	30
5.1 The Mentor Graphics	30
5.2 The Design Architecture	31

CHAPTER 1

INTRODUCTION

One of the greatest revolutions of our age is the advent of the silicon chip. It is now possible to produce a die with over a million transistors on it so that total systems can be produced on a single chip. It is not difficult to imagine the changes that this is introducing to the whole society. A part of this revolution is the drastic change in component costs of a system.

A decade or so ago active electronic components and the assembly of them onto a printed wiring board constituted the major cost of the system. By integrating the complete system into a single component, these costs are considerably reduced and are often dwarfed by the costs of the subsidiary components such as plugs, sockets, interconnecting cables, switches and the box to house it all in.

A further advantage of being able to integrate a total system is the improvement of reliability. As a first order approximation, the reliability of a system is proportional to the number of solder or made connections. By integrating a system onto a single chip there is a considerable improvement in reliability. Chip reliability is extremely high with modern clean rooms and stable fabrication processes. Even if a failure should occur, the fault finding and replacement procedure can be minimal, as the system is basically a single chip, which is simply replaced.