A STUDY ON THE VLSI PARTITIONS :

THE IMPLEMENTATION OF FIDUCCIA-MATTHEYSES

ALGORITHM

Thesis presented in partial fulfillment for the award of the
Bachelor of Electrical Engineering (Hons.) of
MARA Institute of Technology

Burhanuddin Bin Omar
School of Electrical Engineering
MARA Institute of Technology
40450 Shah Alam
Selangor Darul Ehsan

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Acknowledgements

In the name of Allah S.W.T, The Merciful, The Beneficent, The Almighty One. Praised to HIM alone for HIS endowment that let me complete this final year project.

Alhamdullilah , finally the project has been completed within the specified period. I have gained a valuable experience and new knowledge.

Here, I would like to express my personal gratitude to my project advisor, Encik Zulkifli Bin Abd. Majid for his continuous guidance in giving the ideas and assistance in completion of this project. Without his support,ideas and helps, I will never completed on this project.

Special thanks to everybody involved directly or indirectly in this project especially to Encik Kamal Zamli for his assistance and willingness in sharing knowledge and ideas in C programming language.

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Abstract

An iterative mincut heuristic for partitioning networks is presented whose worst case computation time, per pass, grows linearly with the size of the network. In practice, only a very small number of passes are typically needed. To deal with cells of various size , the algorithm progresses by moving one cell at a time between the blocks of the partition while maintaining a desired based on the size of the blocks rather than the number of cells per block. The program is being develop using this algorithm. The evaluation and comparison also been carried out between this method and Kernighan-Lin method.

CHAPTER 1

1.0 Introduction

As 'Very Large Scale Integration', VLSI gets more complex, the design effort and turnaround time increase at a higher rate particularly in the layout design phase. Traditionally, the VLSI design in mainly performed manually. The Z8000 microprocessor was a typical example of such VLSIs. In its design, very little CAD was used. As a result, about 6,600 man-hours, or 50% of the whole design effort, was required in its layout design phase. Altogether, approximately 13,000 man-hours was needed to produce functional / logic / circuit design, mask designs, and testing and characterizing of the resulting design.

As soon as the large scale integration concept emerged at the beginning of the 1960's, CAD was recognized to be indispensable in support of LSI design for the purpose of cutting design effort and turnaround time, eliminating human errors, and as a result, reducing design cost. Since then, various layout design styles and strategies have been proposed : hand-crafted, symbolic, PLA, gate array, standard cell, hierarchical, and so on. There are many factors to be considered in deciding which layout style should be employed. They include design effort and time, packing density, performance (speed, power, noise margin), yield, reliability, etc. There are trade-offs between these factors. In a hand-crafted layout design, maximum flexibility can be used; there is no need for standardization. In order to effectively introduce CAD tools into the design environment,