A STUDY ON THE VLSI PARTITIONS :

THE IMPLEMENTATION OF MINCUT ALGORITHM

Thesis presented in partial fulfillment for the award of the
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Azharul Hisham Bin Abdul Aziz
School of Electrical Engineering
MARA Institute of Technology
40450 Shah Alam
Selangor Darul Ehsan

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Abstract

The term 'Very Large Scale Integration' (VLSI) reflects the capabilities to integrated thousands of transistors in a single silicon chip. As we all know in this computerised era, VLSI becoming very important. Speed, complexity and sizing are the 3 main targets when designing a single chip using VLSI physical design today. There are several techniques to achieve these targets such as partitioning, placement and floorplanning. Here in my project I only discussed about partitioning because this technique itself has a very wide scope. Here I implement Kernighan-Lin Algorithm and make some improvements to it using size and cut sets weighting. The program is being develop using this algorithm. The evaluation and comparison also been carried out between this method and Fiduccia-Mattheyses method.

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CHAPTER 1

1.0 Introduction

The size of present-day computing systems demands the elimination of repetitive manual operations and computations in their design. This motivates the development of automatic design systems. To accomplish this task, a fundamental understanding of the design problem and full knowledge of the design process are essential. Only then could one hope to efficiency and automatically fill the gap between system specification and manufacturing. Automation of a given (design) process requires an algorithmic analysis of it. The availability of fast and easily implementable algorithms is essential to the discipline.

In order to take full advantage of the resources in the very-large-scale intergration (VLSI) environment, new procedure must be developed. The efficiency of these techniques must be evaluated against the inherent limitations of VLSI. Previous contributions are a valuable starting point for future improvements in design performance and evaluation.

Physical design (or layout phase) is the process of determining the physical location of active devices and interconnecting them inside the boundary of a VLSI chip (i.e., an integrated circuit). The measure of the quality of a given solution to the circuit layout problem is the efficiency with which the circuit (corresponding to a given problem) can