SYNTHESIS OF TRANSISTOR- CHAINING ALGORITHM

FOR CMOS CELL LAYOUT

USING EULER PATH

Thesis presented in partial fulfillment for the award of the
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ABSTRACT

The objective of this project is to build Optimal Layout of CMOS Functional Arrays IC standard cell design. Firstly, this report is discussed about the Optimal Layout of CMOS Functional of CMOS functional array.

Optimal Layout is the layout of the arrangment of CMOS transistor with the implementation of a random logic functional on an array of CMOS transistor. After discussing about the introduction (the basic of CMOS transistor), we will discuss how to create the Optimal layout of CMOS Functional Array with the minimum separation based on euler path method. The euler's path it using pseudo input and Heuristic algorithm to find the minimum interlace.

The comparison between euler's path and Bipartite graph Algorithm [14] will be made at the end this of this report to see which one give optimal chaining .

1.0 INTRODUCTION

As the CMOS VLSI technology [1] and the cell based layout methodology get popular, the automatic layout generation of a CMOS function cell becomes very important and attracts attentions from many VLSI/ CAD researches.

In this report, it is proposed that a fast algorithm for the problem of chaining the transistor pairs using minimum number of chains. Input to the algorithm is a CMOS schematic circuit which has equal number of P-type and N-type transistor at transistor level. Output from the algorithm is a minimum set of chain can be realised using only one P-type diffusion strip and N-type diffusion strip once.

By grouping the transistors into pairs with each pair consisting a type and N-type transistor and then model the possible abutments between the pairs using euler's path. Heuristic algorithm is used to find a maximum set of edges which correspond to a maximum number of realisable abutments.