UNIVERSITI TEKNOLOGI MARA

MEMRISTOR SWITCHING MODEL FOR DIGITAL AND ANALOG CIRCUITS

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Thesis submitted in fulfillment
of the requirements for the degree of
Master of Science

Faculty of Electrical Engineering

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CONFIRMATION BY PANEL OF EXAMINERS

I certify that a Panel of Examiners has met on 13th January 2016 to conduct the final examination of Siti Musliha Ajmal Binti Mokhtar on her Master of Science thesis entitled "Memristor Switching Model for Digital and Analog Circuits" in accordance with Universiti Teknologi MARA Act 1976 (Akta 173). The Panel of Examiners recommends that the student be awarded the relevant degree. The panel of Examiners was as follows:

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AUTHOR'S DECLARATION

I declare that the work in this thesis was carried out in accordance with the regulations of Universiti Teknologi MARA. It is original and is the results of my own work unless otherwise indicated or acknowledged as referenced work. This thesis has not been submitted to any other academic institution or non-academic institution for any degree or qualification.

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ABSTRACT

Scaling of complementary-metal-oxide-semiconductor (CMOS) transistor for higher performance device is nearly reaching its limit due to technology limitation issues. In this research, main objective is to incorporate a nanodevice called memristor into CMOS circuit as one alternative to overcome scaling limitation due to memristor fabrication is compatible with CMOS. The first requirement in this research is to develop SPICE model for memristor in circuit simulation. Research starts with model selection and validation through comparison with fabricated memristor sample followed by model development in LTSPICE. In this research, memristor applications are investigated from both digital and analog memristor resistance switching. For digital, memristor-based logic modules are invested. For analog, a novel design of programmable delay element (PDE) using memristor is proposed. A case study of implementing the proposed PDE in delay locked loop (DLL) is also discussed. For model development, OSM model is validated and has most comparable behavior with sample. Next, hybrid memristor-based logic gates (AND, NAND, OR, NOR) designs and operation results are discussed. They showed similar operation with CMOS logic. Hybrid XOR shows 88% less area consumption compared to fully CMOS XOR thus supports the main objective. However, hybrid logics have dynamic behavior at output caused by slow memristor switching speed. Speed can be increased through thinner thin film and higher voltage supply. Finally, the proposed PDE showed delays that are programmed by adjusting memristor resistance. Case study of DLL proved proposed design functionality in more complex system. However, it consumes more area than CMOS DLL.

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